AREA EFFICIENT VLSI BASED ROUTER

[1]Dr. D. David Neels Ponkumar, [2]V. Sushmitha
[1]Associate Professor/ECE, [2]PG Scholar – VLSI design,
[1,2]Dr. Sivanthi Aditanar College of Engineering,
[1]david26571@gmail.com, [2]sushmithav1195@gmail

Abstract
An area efficient VLSI based Router is designed using the Verilog modules and a detailed study of FIFO usage in it is analysed. The design entry of these router is done using Verilog. Their corresponding test fixtures are synthesized and implementation of the design are obtained using Xilinx ISE Design Suite 14.3. And on chip power consumptions are obtained using XPower Analyzer Tool. The functionality verification of the router is obtained in the form of simulation waveform results from ModelSim -Altera 6.5b. Upon analysis, it is found that the FIFO in a complete design of VLSI based router plays a major role in routing as well as using it an area efficient router is designed.

Keywords: Area utilized, MPSoC, NoC, Networking, On Chip Power, Registers.

I. INTRODUCTION

The driving force behind Integrated Circuit (IC) technology has been Moore's law for almost five decades. Although this is projected to slow down to doubling every 3 years in the next few years for fixed chip sizes, the exponential trend is still in force. Because of the evolution, the system level focus moves in steps. It leads to a paradigm shift through the technologies maturity for a given implementation style. Past examples of such shifts were moving from room- to rack-level systems (LSI-1970s) and later from rack- to board-level systems (VLSI-1980s). This trend allowed in the 1990's the introduction of Systems on-Chip (SoC), the integration of many components such as Microprocessors, custom IP, and even analog in a single die. The integration of many processing and memory cores in a single chip introduced in turn a communication overhead that traditional bus-based architectures cannot handle for a number of reasons. More specifically the interconnection infrastructure has a significant impact on SoC costs. In order to solve the problems, NoC (Network-on-chip) is a good paradigm. NoC is an integrated network that uses routers to allow the communication among those blocks. It uses networking theory methods for on-chip communication so that the blocks can exchange information on a chip just like what the terminals do in the actual world.

II. NETWORK ON CHIP

NoC technology is a new approach to communication that enables not only more efficient interconnects but also more efficient design and verification processes for modern SoCs. NoC is an efficient approach to signalling that matches the needs of the signal to various communications in a way that reduces the complexity of the chips interconnect. A typical NoC-based MPSoC is composed of a number of components, called *nodes*, including Processing Elements (PEs), such as CPUs, custom IPs, DSPs, etc., and storage elements (embedded memory blocks).

A. ROUTER DESIGN

Router architectures have dominated early NoC research by Concatto et al (2009) and the first NoC designs proposed the use of simplistic routers, with deterministic routing algorithmsIn terms of RTL design, since the router is a component that is very likely to be used in future versions of the system, and its architecture options may be either revised or even different instances may coexist in the same architecture (heterogeneous NoCs), it should be designed as a reusable IP block. The design of VLSI based Router is shown in the figure2. It consists of three major components such as

- Buffer
- Arbiter unit
- Registers

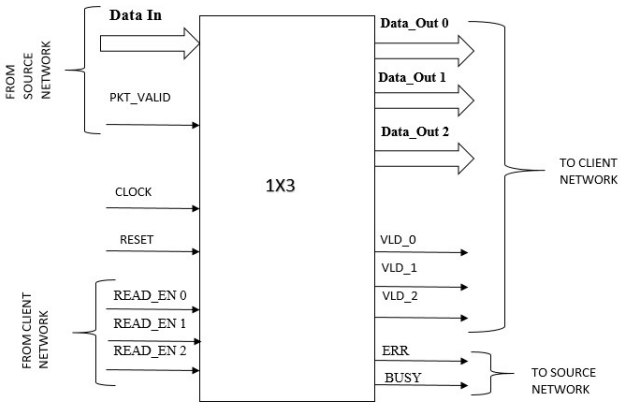

Fig. 1. VLSI based Router Design

B. BUFFER

Buffers are the greatest power consumers. Thus, efficient buffer design is critical for achieving a good performance, area, power trade-off. To minimize the implementation cost, the on-chip network has to be implemented with little area overhead. Thus, unlike off-chip networks which feature large memories, often DRAMs, NoCs typically use small registers for buffering. Another advantage of using registers over large memories is that the address decoding/encoding latency and the access latency can be significantly reduced. The design of FIFO which has to be fit inside the Router is designed. There are 3 FIFOs used in these router design. Each FIFO used here is of 9 bits wide and 16 bit bytes depth. The FIFO works on the system clock and it will reset with a synchronizer active low reset.

C. ARBITER UNIT

The arbitration in these router is done using FSM logic .Finite state machine in general is simply another name for sequential circuits. Finite refers to the fact that the number of states the circuit can take finite. A synchronous clocked FSM changes state only when a triggering edge occurs on the clock signal. It provides the selection process of selecting the operation to be carried out by the router. Then followed by the synchronizer.

III. RESULTS AND DISCUSSION

The design of VLSI based Router is done using Xilinx ISE software. The design is simulated using Model Sim .

The Schematic diagram of basic Buffer is shown in figure 2.The working of the buffer takes place at every rising edge of the clock as well as when the enable signal is at HIGH logic.

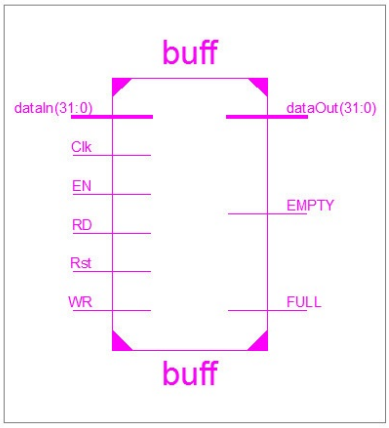

Fig 2, Basic Buffer

Upon Simulation of Buffer module it is found that the data input word 1010101010101010 is read at the data out port when the read signal of the buffer is at HIGH logic.

The Schematic diagram of basic buffer with indication of full and empty is shown in figure 3.The output of these type of buffer is designed in such a way to show the availability of buffer space such as one space, two space and no space so that it can be used for reuse of slots.

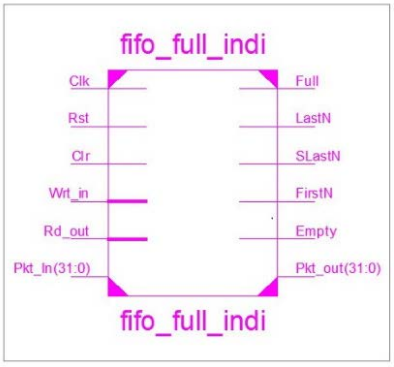

Fig 3, Basic Buffer with indication of full and empty

The Buffer compatible for the router is designed using the write enable, read enable, soft reset and load first data as the control signals the schematic diagram of FIFO in Router is shown in figure 4.

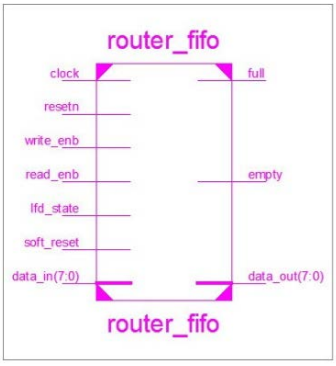

Fig 4, FIFO in Router

The simulation waveform of FIFO within the Router is shown in figure 5.

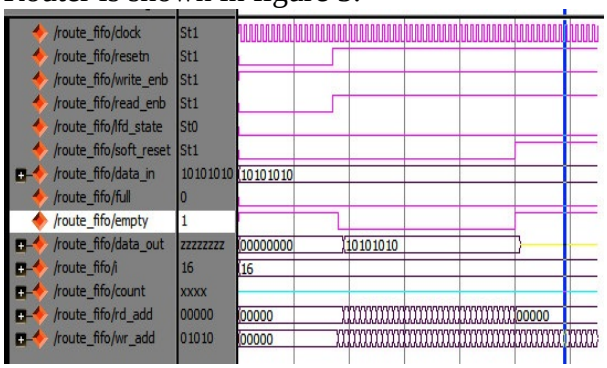

Fig 5, Simulation waveform of FIFO within the Router

The Schematic diagram of VLSI based Router is shown in figure 6.

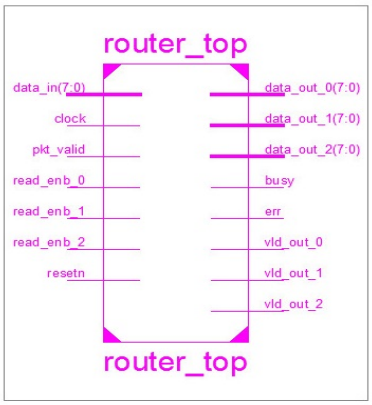

Fig 6, Schematic diagram of VLSI based Router

The router works based on the validity of the packet valid signal and read enablesignal. The Simulation waveform of VLSI based Router is shown in the figure 7.

Fig 7, Simulation waveform of Router

The above simulation results indicates that there is a valid out request is from FIFO 0 but the read enable of FIFO 2 is activated and the data out of FIFO 2 provides the wrong packet .so that, the error signal is high indicating there is a error in the routing .although there is error still the FIFO is holding some packet value, it is indicated by high value of the busy signal.

The FIFO in a complete design of VLSI based routerconsumes power of 0.05mW, logic power of 0.02mW, signal power of 0.03mW at 50MHz frequency which is lesser than the power consumption of the buffer and FIFO s designed using Verilog.

The area utilisation of the router designed is obtained from the design summary report and it is found that it occupies a less area as shown in the below figure 8.

Device Utilization Summary				
Slice Logic Utilization	Used	Available	Utilization	N
Number of Slice Registers	25	11,440	1%	
Number used as Flip Flops	24			
Number used as Latches	1			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	38	5,720	1%	
Number used as logic	38	5,720	1%	
Number using O6 output only	25			
Number using O5 output only	0			
Number using O5 and O6	13			
Number used as ROM	0			
Number used as Memory	0	1,440	0%	

Fig 8, Device utilization summary

IV. CONCLUSION

In this paper, the VLSI based Router is designed using the FIFO, Arbiter Unit and a detailed study of FIFO usage in it is analysed. The design entry of these router is done using Verilog. Their corresponding test fixtures are synthesized and also the implementation design are obtained using Xilinx Ise Design Suite 14.3 and their corresponding Power consumptions are obtained using XPower Analyzer Tool. The functionality verification of the router is obtained in the form of simulation waveform results from ModelSim -Altera 6.5b. Upon analysis, it is found that the FIFO in a complete design of VLSI based router plays a major role in routing as well as using it an area efficient router id designed.It consumes about 95.3% of total on chip power consumption at 50MHz frequency.

REFERENCES

[1] A.Hemani, A.Jantsch, S.Kumar, A.Postula, J.Oberg, M.Milberg and D.Lindqvist, (2000), “Network on chip: Architecture for billion transistor era”. In Proceeding of the IEEE Nor chip conference.

[2] Amit Bhanwala, Mayank Kumar and Yogendera Kumar(2015), “FPGA based Design of Low Power Reconfigurable Router for Network on Chip

(NoC)".International Conference on Computing, Communication and Automation2015, IEEE 1320.

[3] Ben-Itzhak, Y., Cidon, I., Kolodny, A., Shabun, M., &Shmuel, N. (2015), "Heterogeneous NoC Router Architecture" . IEEE Transactions on Parallel and Distributed Systems, 26(9), 2479–2492.

[4] Concatto, C., Matos, D., Carro, L., Kastensmidt, F., Susin, A., &Kreutz, M. (2009), " NoC Power Optimization Using a Reconfigurable Router". IEEE Computer Society Annual Symposium on VLSI.

[5] DeboreMatos,CarolineConcatto, Luigi carro, Fernanda Kastensmidt and MaccioKreutz,(2015), " Highly efficient Reconfigurable Routers in Network-on-Chip".IEEE Transaction on Very Large Scale Integration (VLSI) Systems

[6] Deepak S, Divyaprabha, M Z Kurian (2015), "Design and Verification Of Network-On-Chip Router Architecture". International Journal of Advanced Computational Engineering and Networking, ISSN: 2320-2106, Volume-3, Issue9.

[7] Gaurav Verma ,Harsh Agarwal, Shreya Singh,ShaheemNighatKhanam,Prateekkumar Gupta and Vishal Jain,(2016), "Design and implementation of router for NOC on FPGA", International Journal of Future Generation communication and networking Vol.9.No.12(2016),pp.263-272

[8] Kumar, S., Jantsch, A., Soininen, J.-P., Forsell, M., Millberg, M., Oberg, J., Hemani, A. (n.d.).(2002), "A network on chip architecture and design methodology", Proceedings IEEE Computer Society Annual Symposium on VLSI. New Paradigms for VLSI Systems Design. ISVLSI 2002.

[9] Li, X., Duraisamy, K., Baylon, J., Majumder, T., Wei, G., Bogdan, P.,Pande, P. (2017), "A Reconfigurable Wireless NoC for Large Scale Microbiome Community Analysis". IEEE Transactions on Computers, 66(10), 1653–1666.

[10] Meenu Anna George, Aravindhan and Lakshminarayanan(2017),"Design of five port priority based router with port selection logic for noc". ICTACT Journal On Microelectronics, Volume: 02, Issue: