IMPROVED MULTILEVEL INVERTER WITH NEUTRAL POINT POTENTIAL BALANCING FOR HIGH POWER APPLICATION

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Abstract—This paper presents low harmonic distortion andneutral-point potential (NPP) balancing in multilevel inverter using multicarrier pulse width modulation (PWM) for medium-voltage high-power industrial ac drives. This method is applicable for five-level inverters or higher. A high performance of the machine is observed experimentally at low switching frequency operation employing the proposed technique. In the past, low distortion and optimal common-mode voltage at low-switching-frequency control have been reported using proposed synchronous optimal PWM.

Index Terms—Multilevel inverters, neutral-point potential (NPP) balancing,medium-voltage drives, carrier based pulse width modulation (CBPWM).

I. INTRODUCTION

Ac drives have found applications in high-power industrial applications, including oil plant and gas plantsectors, production plants, and process industries. To get the better efficiency at higher power, the voltage rating, rather than the current of the inverter, is increased to limit the conduction losses. Multilevel inverters can achieve higher level of voltage without the need of a transformer while keeping the voltage stress across the devices to half, low *dv/dt*of the output voltage, and low harmonic distortion, low electromagnetic interference, this resulting in low total harmonic distortion (THD), they gives attractive solution to high-power ac drives [2]–[4].A selective harmonic elimination (SHE) technique used to calculate the switching angles for eliminating harmonics. A generalized SHEtechnique for two-level single-phase and three-phase invertersto eliminate a fixed number of harmonics was first explainedand reported in [5] and [7] in the Fourier domain. Programmedharmonic elimination, which is an extension of previously reported SHE technique has been proposed in [8] and[9]. It develops optimal pulsewidth-modulated (PWM) structureto reduce harmonic distortion. A similar SHE techniqueusing a Walsh function to express the harmonic amplitudes ofthe inverter output voltage and current as functions of switching angleshas been reported [9], [10]. Fast transient response and efficient harmonic filteringis proposed in [11]. Solution proposed in [12] converts thetranscendental equations that specify the harmonic eliminationproblem into an equivalent set of polynomial equations tofind the switching angles that produce the fundamental whilenot generating specifically chosen harmonics. The complete solutions for both unipolarand bipolar switching patterns to eliminate the fifth andseventh harmonics are presented.

Quarter-wave symmetric restricts the solution space,
This may result in suboptimal solutions with regard to
the uncontrolled harmonic distribution, and is not strictly necessary. Amore general formulation is proposed, removing the quarterwavesymmetry constraint for harmonic control problems [14].Space vector modulation (SVM) is considered a powerful techniqueto impose low harmonic content in machine windingsif the switching frequency is around 1 kHz or higher. UsingSVM at low switching frequency leads to unacceptable highharmonic distortion of the machine currents.Optimized

SVM, which is a modification to conventional SVM, has been reportedto minimize THD and to improve the performance of the motordrive. However, this technique is based on switching frequencyhigher than 1 kHz. A method to derive complete results forthe bipolar SHEPWM for both single-phase and three-phaseconverters has been presented in [15]. Multiple sets of solutionspresenting an independent solution to the same problememploying SHEPWM for inverter control exist, and certainsets may offer an improved overall harmonic performance. Aminimization method is discussed as a way to obtain thesemultiple sets of switching angles [16]. An alternative realtimeSHE method based on modulation is presented in [17].A modified triangle carrier is identified, which is comparedwith an ordinary sine wave. In place of the conventionaloffline solution of switching angles, the process simplifies togeneration and comparison of the carrier and sine modulation,which can be done in minimal time without convergence orprecision concerns. The method does not require an initialguess. In contrast with other SHE methods, the method doesnot restrict the switching frequency to an integer multiple ofthe fundamental. A low-frequency square-wave inverter witha series-connected PWM inverter is discussed for high-powerapplications [18]. The series compensators produce only thedesired harmonic voltages to make the net output voltagesinusoidal with small PWM switching harmonics only. Thenet output voltage only has the fundamental component withrelatively small switching harmonics [18]. However, switchinglosses of power semiconductor devices at the medium-voltagelevel still remains a concern. Using higher switching frequencyreduces harmonic distortion but increases the switching lossesand reduces the inverter efficiency. Multicarrier PWM for low-switchingfrequencycontrol of medium-voltage multilevel inverters whilemaintaining low THD has been reported in [18]–[21]. Thistechnique permits reducing the switching frequency down to20% without sacrificing harmonic content. It has been demonstratedin [18]–[21] that device switching frequency below200 Hz can be combined with lowharmonic distortion in the machinecurrents. Reducing the switching frequency reduces theswitching losses and thus increases the efficiency of the inverter. Using CBP, low distortion of machine currents and optimalcommon-mode voltage (CMV) in single dc link topology havebeen reported [22]. However, the neutral-point potential (NPP) balancing issue was never reported with the proposed SOPmodulation [21], [22] but was focused on minimizing THD [21]and CMV [22]. The NPP is an important problem and has beenattended in this paper. A simple and easy approach using CBP to address this issue has been proposed. The objective of thispaper is to explain and experimentally demonstrate the NPP balancing using CBP modulation. This paper first introduces the CBP and then the NPP balancing methods while adopting CBP in five-level inverters or higher. Note that *NPP balancing*means voltage balancing of the input split capacitors in neutralpointconverters .Fig.1 shows two different five-level inverter topologies withisolated dc links and a common dc link. Defining a five-levelinverter waveform offers an additional degree of freedom aftereach logic level $l = 1$, i.e., the potential of either $l = 2$ or $l = 0$can be chosen. Similarly, after $l = -1$, $l = 0$ or -2 can bechosen. Depending on the switching state of that phase, theinverter output potential per phase can acquire five discretelevels, i.e., $-ud$, $-ud/2$, 0, $+ud/2$, or $+ud$, to which the logiclevels $l = -2, -1, 0, 1,$ and 2 are associated, respectively.This paper has been organized as follows. Generalized multicarrier PWM control is discussed in Section. II. NPP balancing mechanismsare explained in Section III. Simulation circuit IV. Experimental results are demonstrated.

II. SWITCHING PATTERNS

In this method, the pulse patterns (sets of switching angles)are calculated offline, assuming a steady state of the drive.The switching frequency is synchronized with the fundamentalfrequency of the voltage waveform [18]–[21]. The number of switching angles over a quarter of the fundamental period, which is called a pulse number, is therefore an integer, i.e.,

$$N=\text{floor}\left(\frac{(L-1).f_{s,max}}{2.f_1}\right) \qquad (1)$$

where floor generates an integer value. f_s,maxis the maximum switching frequency, f_1 is the fundamental frequency of the voltage

waveform, , and L and L is the number of inverter logic levels in the inverter, i.e., L = 3 for a three-level inverterL= 5 for a five-level inverter, etc. Depending on which combination of choices is taken, several possible "*structures*" and, therefore, several inverter-phase potential waveforms for given values of m and N exist.

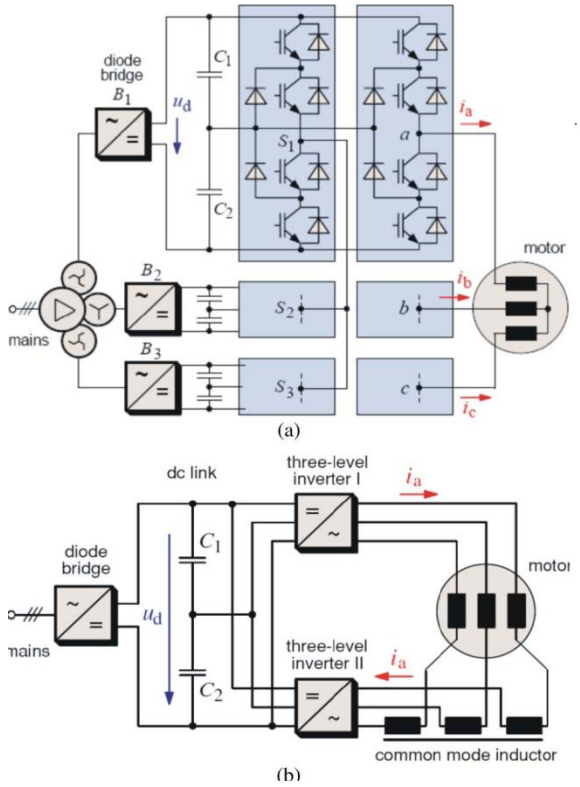

Fig. 1.Five-level inverter configurations. (a) Series connection of two threelevelhalf-bridges per phase. (b) Series connection of two three-level inverters.

$$n_{st} = 2\text{floor}(N/2) - 1 \qquad (2)$$

For example, at N = 7, the number n_{st} of inverter outputpotential waveforms or possible structures is n_{st} = 7, as shownin Fig. 2(b) over a quarter period. The modulation index m canbe also represented by a ratio of fundamental frequency $f1$torated fundamental frequency $f1R$, which is given by

$$m = \frac{f_1}{f_{1R}} \qquad (3)$$

At rated fundamental frequency $f1R$,m= 1, and the inverter shows a six-step operation. From (1) and (3), the pulse number can be also defined as

$$N = \text{floor}\left(\frac{(L-1).f_{s,max}}{2.f_1}\right) \qquad (4)$$

It is clear from (4) that once setting the maximum switching frequency to a desired low value, pulse number N (number of commutations or switching angles) increases at lower values of modulation index m, i.e., reduction in stator fundamental frequency $f1$. Therefore, it increases the number of possible structures n_{st} as in (2).

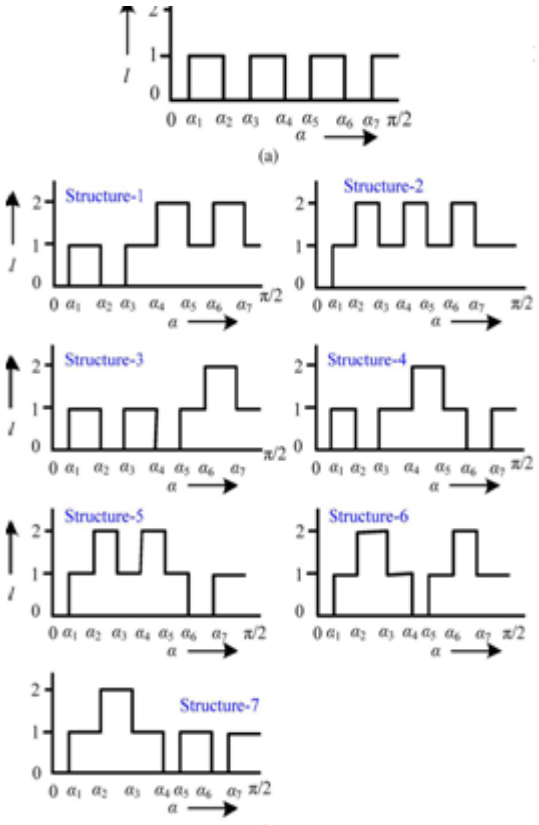

Fig. 2.Multilevel waveforms per quarter wave. (a) Three-level waveform.
(b) Five-level waveforms defined for N = 7. Logic level l = 1 correspondsto$ud/2$ and l = 2 to ud

Fig. 2 shows the growth in the number of structures witha pulse number. We have n_{st} = 32 at N = 10, n_{st} = 1023at N = 20, and n_{st} = 2045 at N = 22. Different structures produce different values of distortion d. If the modulation index mis lower, the pulse number $N$and the number of possiblestructures n_{st}will be higher; therefore, the computation timewill be also higher. The computation time is significant inthe laboratory environment with one computer, albeit modernfast, and advanced.

However, in industries with several CPUs (higher CPU strength with advanced computational software),it is no longer critical or serious. The structure with the lowest distortion and continuities in angles is selected [18]–[25].Discontinuities in switching are avoided to achieve a bettertransient response. The dynamic losses of the semiconductordevices are reduced by restricting the switching frequency toa maximum value, i.e., $f_s \leq f_{s,\max}$. The switching anglesover a quarter of the fundamental period are optimized foreach steady-state operating point using a gradient method thatintroduces the least distortion [21], [22].Half-wave and quarter-wave symmetries are introduced to eliminate even-order harmonics.Therefore, calculation over aquarter of the fundamental period needs to be done to define theswitching angles αi, $i = 1, 2, \ldots, N$. By symmetry, the anglesof a full cycle are generated after optimization.Fig. 2b shows the division of five-level potential $V5L$ into twothree-level potentials $V3L-1$ and $V3L-2$ for $N = 7$. Eight threelevels*witching patterns* are possible, as shown in Fig. 2. It isselected such that the constituent two three-level half-bridgeshare equally loaded, sharing equal losses, producing symmetricalvoltage waveforms, and avoiding short voltage spikes/notches,i.e., avoids any very close two consecutive commutations. Judgingbased on the aforementioned criteria, a second *switchingpattern* is selected. With $N = 7$ being an odd pulse number,one three-level half-bridge operates at $(N - 1)/2$ and the otherat $(N + 1)/2$.The switching patterns of the two three-level half-bridgeshare interchanged either in the next half cycle or after a fullfundamental period to retain symmetry and sharing load andlosses equally, as shown in Fig. 2.Even for an even pulse number N, due to different conductiontime (pulse duration) for the two three-level inverters,the pulse patterns between two three-level half-bridges areswapped after every fundamental period or half cycle to balancethe conduction losses and maintain equal load sharing. It also results in thermal balance.

III. NPP BALANCING

Voltage balancing is necessary to the inverter.Based on the modulation index more impact is there on the several patterns.It gives considerable impact on ripple produced at dc link. Dc link capacitors are connected to the circuit. The voltage difference between the two phase must be very less. The losses introduce the unbalance in the output of the inverter. This gives unbalance output therefore in machine current also. Therefore, the multi carrier pulse pattern may not result in minimal d without accounting this condition of the dc link ripple. The dc link ripples produce distortion in output waveform. Therefore this condition should be satisfied with N number of levels. Unbalance in dc link is more common, but we have reduce this unbalance voltage. There are more number of methods are available for reducing the harmonics here we used neutral point potential balancing. In that several neutral point balancing methods available. It leadsto an incorrect volt-seconds, which influences the incorrect modulation of ($\Delta unp = uC1 - uC2$) balancing. It gives incorrect modulation of output, so the output hence create the changes in motor parameter also like current, speed and also in torque also. And it also lead to unstable operation of inverter. Furthermore an excessive NPP may imposes the error and voltage stress. A seven level inverter may an medium level ($+ud/2, -ud/2$) can be imposed by eitherusingthe positive capacitor voltage ($+ud/2+, -ud/2+$) with respectto the neutral point$N$or the negative ($+ud/2-, -ud/2-$). Consideringnonzero output voltage only in phase a, e.g., switchingstate $S+ = \{+ud/2+\ 0\ 0\}$, the neutral-point current $i$npisequal to thephase current ia. On the contrary, the switchingstate $S- = \{+ud/2-\ 0\ 0\}$, which imposes the same voltage atthe machine terminals, leads to $inp = -ia$. This shows that the redundant levels ($+ud/2+, +ud/2-$) and ($-ud/2+, -ud/2-$)have a direct effect on the neutral-point current and henceinfluence the NPP.

A. NPP Balancing by multicarrier PWM

The calculated five-level patterns by carrier based pulse width modulation are divided intotwo three-level patterns and swapped the losses are balanced periodically and to maintain equal load sharing [4] in all situation..Thereby, the redundant medium levels ($+ud/2+, +ud/2-$) and($-ud/2+, -ud/2-$) are periodically used in each phase. Thus,at a steady-state operation, the NPP balancing is aslong as the losses are balanced between the two half-bridgesof each

inverter phase. However, a small ripple exists, and themechanism is slow.

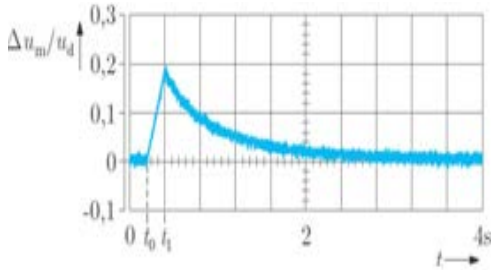

Fig. 3.Natural balancing of the NPP.

IV.SIMULATION CIRCUIT

Simulation is the better way to establish the system and is its efficiency. Fig 4 shows the seven level multilevel inverter shown with neutral point potential balancing done by use of spilt capacitor. In this circuit N=7 and the losses reduced very effectively.The next section shows result of the seven level inverter system with motor parameter.

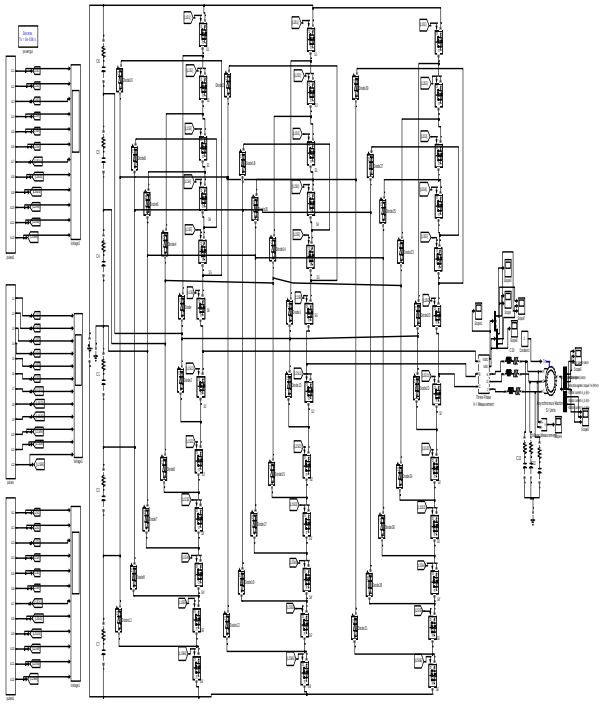

Fig.4.Simulation circuit of seven level multilevel inverter

EXPERIMENTAL RESULTS

The carrier based control of an induction motor drive was tested using a seven-level inverter. Switching angles calculated using computer programming were stored in a microcontroller. The switching states of the devices were programmed. The following Fig 5 shows the voltage and current waveform of seven level multilevel inverter.

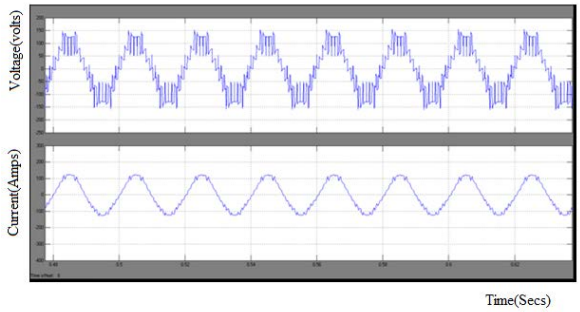

Fig 5.Voltage and current waveform of seven level inverter output

If we connected the system in three phase the three phase output will be delivered.the Fig.6 represent the sevel level inverter which connected in three phase and the voltage waveform three phase multilevel inverter is shown

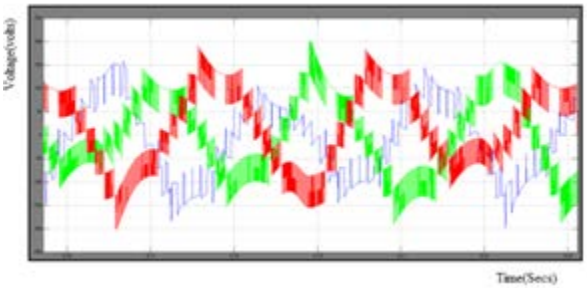

Fig .6.Voltage waveform of three phase multilevel inverter

Then the inverter can also perform with the load.The load can be any kind of ac drive. The induction motor is here connected as load. The performance of induction motor had been improved because of this neutral point potential balanced multicarrier inverter. It performance has been shown by the following graph. Fig.7 shows torque, speed, current output parameter of the motor.

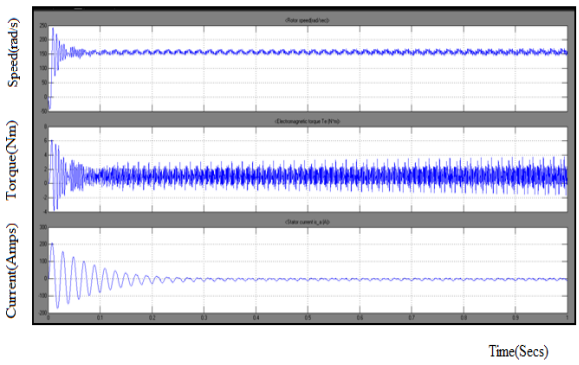

Fig.7.Induction motor current,speed,torque parameter

The above graph represents the induction motor current,speed,torque.Here speed of the motor increased very well it extends to 1645rpm and the current stabled in 5amps.Torque also stable in this system. Voltage balanced by the use of neutral point potential balancing.

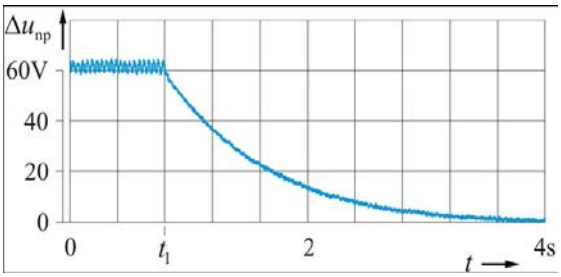

Fig. 8. Natural balancing of NPP error (m = 0.6,N= 10, fs= 280 Hz).

Fig 8 represents the NPP balancing error .It is found at Experimental results and 9 for m = 0.78 and N = 5, and for m = 0.65 and N = 6, respectively.An insulated-gate-bipolar-transistor-based seven-level inverter is used. The dc link voltage ud= 320 V, and the maximum output power of inverter = 30 kVA.
The phase potentials of two three-level half-bridges per phase V3L−1 and V3L−2, the five-level inverter V5L, and the machine phase current $ia$are shown in the Fig 9.

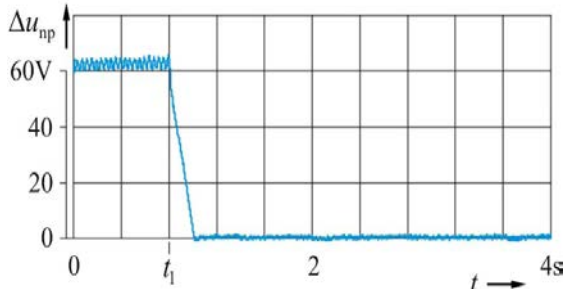

Fig. 9. Behavior of the NPP error at redundant half-bridge control (m = 0.6and N = 10).

Similarly, $Sb$is used for phase b, and $Sc$is used for
Phase$c$. They are simple logic signals built in a digital platformwith fundamental frequency and 120◦ phase shifted for otherphases. It is a simple implementation. Signal $So$is not agenerated signal. It is not applied. It is simply a measure oran observation. It has been observed that $So$is a measure of theNPP ripple.An experimental measurement of the control capability, asdiscussed earlier, for the operation point (m = 0.6,N= 10) isgiven in Fig. 13. At time instant t1, the control algorithm forthe NPP is activated. The NPP error decays to zero within about200 ms. Multicarrier PWM results in minimum harmonic distortion at low switchingfrequency provided that steady-state conditions prevail. Thedynamic modulation error appears instantaneously at changesof operating conditions; it increases the harmonic content.Frequent changes of the operating point may generate multipledynamic modulation errors. Transient conditions, however,interfere adversely with the optimal modulation patterns. Trajectorytracking control is employed to achieve high dynamiccontrol in conjunction with multicarrier PWM[18], [19], [27]. An optimaltrajectory of the stator flux linkage vector is derived from thepulse pattern in actual use. The stator flux linkage vector isforced to follow this target trajectory. Modifying the targettrajectory in transient conditions enables closed-loop torquecontrol in a deadbeat fashion while conserving optimal modulation[18], [19], [27].

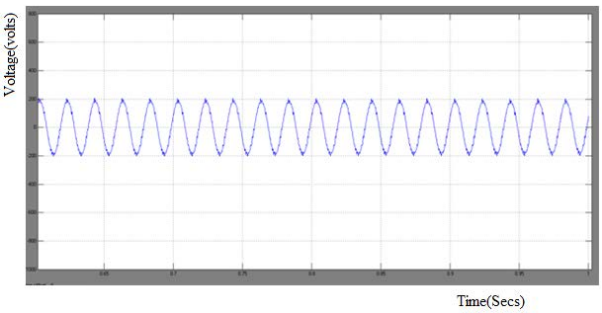

Fig.10.Filtered output of seven level inverter

The above Fig.10 shows the filtered output of seven level multilevel inverter. The figure shows waveform similar to sinusoidal waveform because it is free from harmonic distortion.

V. SUMMARY AND CONCLUSION

This project presents the performance of multilevel converter. The simulation results are in close agreement. We can observe that the quality of voltage and current waveforms increases with voltage level. The notches in the current and voltage waveforms reduce with increase in voltage level. Thus comparing the results it is observed that harmonic content has been predominantly reduced and drives performance improve. A new basic neutral point potential balancing(NPP) for the multilevel converter has been proposed.. The

proposed topology extends the design flexibility and the possibilities to optimize the inverter for various objectives. It has been shown that the structure, consisting of NPP with multilevel inverter has the minimum number of switches for a given number of voltage levels. It has been shown that the proposed topology provides 7 levels on the output voltage. The proposed topology not only has lower switches and components in comparison with other one, but also it gives reliable and effective voltage. Reduction of the Power losses and harmonics of the proposed topology is another advantage of the proposed converter. The proposed topologycan be a good solution for applications that require high power quality, or applications that have considerable numbers of dc voltage sources. The simulation for the existing and proposed was done by using the MATLAB/Simulink. The various voltage and current waveforms are also verified. In future the increased levels in neutral point potential balancing multilevel inverter can done and the simulation results for various voltage and currents.

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