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&
6th International Conference on Progress In Production, Mechanical And Automobile Engineering (ICPMAE 2015)

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Editor-in-Chief

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About Conference

Technical Research Organisation India (TROI) is pleased to organize the 6th International Conference on Computer Science and Information Technology (ICCIT 2015), 6th International Conference on Innovations In Electrical and Electronics Engineering (ICIEEE2015) & 6th International Conference on Progress In Production, Mechanical And Automobile Engineering (ICPMAE 2015)

ICCIT is a comprehensive conference covering the various topics of Engineering & Technology such as Computer Science and IT. The aim of the conference is to gather scholars from all over the world to present advances in the aforementioned fields and to foster an environment conducive to exchanging ideas and information. This conference will also provide a golden opportunity to develop new collaborations and meet experts on the fundamentals, applications, and products of Computer science & IT. We believe inclusive and wide-ranging conferences such as ICIEEE can have significant impacts by bringing together experts from the different and often separated fields of Electrical & Electronics. It creating unique opportunities for collaborations and shaping new ideas for experts and researchers. This conference provide an opportunity for delegates to exchange new ideas and application experiences, we also publish their research achievements. ICIEEE shall provide a plat form to present the strong methodological approach and application focus on Electrical & Electronics engineering that will concentrate on various techniques and applications. The ICPMAE conference cover all new theoretical and experimental findings in the fields of Mechanical, Production & Automobile engineering or any closely related fields.

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TABLE OF CONTENTS

SL NO	TOPIC	PAGE NO

Editor-in-Chief

I.Hameem Shanavas

Editorial

The conference is designed to stimulate the young minds including Research Scholars, Academicians, and Practitioners to contribute their ideas, thoughts and nobility in these two integrated disciplines. Even a fraction of active participation deeply influences the magnanimity of this international event. I must acknowledge your response to this conference. I ought to convey that this conference is only a little step towards knowledge, network and relationship.

The conference is first of its kind and gets granted with lot of blessings. I wish all success to the paper presenters.

I congratulate the participants for getting selected at this conference. I extend heart full thanks to members of faculty from different institutions, research scholars, delegates, TROI Family members, members of the technical and organizing committee. Above all I note the salutation towards the almighty.

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ULTRASONIC SMART CANE INDICATING A SAFE FREE PATH

TO BLIND PEOPLE

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Abstract- Any individual with limited or no sight is a disadvantage in today's society. Walking safely and confidently without any human assistance in urban or unknown environments is a difficult task for blind people. Throughout the world, there are approximately 39 million individuals who are totally blind plus an additional 284 million who are visually impaired. Persons who are blind and deaf frequently suffering when exercising the most basic things of daily life and that could put lives at risk while traveling,Visually impaired people generally use either the typical white cane or the guide dog to travel independently. The white cane is a widely used mobility aid that helps visually impaired people navigate the surroundings. Although the white stick gives a warning about 1 m before the obstacle, for a normal walking speed of 1.2 m/s, the time to react is very short (only 1 s). The idea of this research in the design and manufacturing ultrasonic sensor handheld combines the properties of sound monition and that benefit the blind and vibrating alert feature, which benefit from the experience of deafness. Sensor can detect obstacles within the designed range to avoid the blind person through the issuance of distinctive sound or vibration can be issued by the sense of the deaf by putting his finger on the button at the top of the device vibrate when there is a risk.

Keywords: AVR, Vibration Motor, Ultrasonic (Srf05) Sensor, IR, voice alert .

1. Introduction

Figure 1.1 Blind Person

The work we present in this paper is based on the use of new technologies to improve visually impair people mobility. Our research focuses on obstacle detection in order to reduce navigation difficulties for visually impaired people[1]. Moving through an unknown environment becomes a real challenge when we can't rely on our own eyes, The common way for navigating of visionless person is using a white cane or walking cane. The walking cane is a simple and purely mechanical device dedicated to detect static obstacles on the ground, uneven surfaces, holes and steps via simple tactile-force feedback[4]. However, this cane does not allow sufficient exploration of objects that are at the top or which are getting too closer. The stick

scans the floor and consequently cannot detect certain obstacles (rears of trucks, low branches, etc.). Safety and confidence could be increased using devices that give a signal to find the direction of an obstacle-free path in unfamiliar or changing environments.

2. Literature survey

Electronic travel aids (ETAs) are devices that give off a warning by auditory or/and tactile signals when an obstacle is in the way and allow the user to avoid it. Several devices have been developed to improve the mobility of blind people [3], [4]: talking GPS [5], devices for landmark identification (near-infrared (IR) light or radio frequencies) [6], [7], ultrasonic obstacle detectors (K sonar[8], Ultracane[9], Miniguide[10], Palmsonar [11], Ultra-Body-Guard [12], and iSonic cane [13]), and optical devices (the laser long cane [14]). In indoor or outdoor crowded environments, ultrasonic devices are limited due to multiple reflections [4]. The major disadvantages of these solutions are:

1) They only detect obstacle existence and distance without specifying indication about their nature which is important for the user to know.

2) They are unable or inaccurate in detecting some obstructions that are not protruding but present potential threat such as descending stairs, holes, etc.

3) The system communicates its recommendations, through intensity or frequency variations. Thus feedback information is often sent to the user through vibration or sound signals. So a training course is needed to keep the user informed about how to understand and react in real time to alerts that are transmitted regarding the existence of obstacles as well as their recognition. On the one hand, such training can be sometimes more expensive than the product itself. On the other hand, it is often difficult and complex for the users to assimilate it properly. Furthermore, in the case, where information is transmitted as an acute sound, that may happens several times especially when the obstacle is very close, it

may be embarrassing for the blind person when they are in public. Therefore, our interest is specifically focused, on the development of an electronic tool using two types of sensors which are ultrasonic sensors and monocular camera. Our choice of these sensors takes into account theirs area of operation and their performances. Our choice also depends on several other factors as: cost, type of scene, type of obstacle to be detected, detection range and desired precision of the measurements. The main idea consists in merging data provided by the two sensor types to allow more accurate information, to be transmitted to the user via a Bluetooth module as a voice message specifying the object nature, characteristics and the distance between the detected obstacles and the device. In this paper, we explore ultrasonic sensor potentials in object detection and mainly stairs recognition. This type of sensors has significant potential in robotic applications. Indeed, it has been widely used in collision avoidance systems and in localization and navigation of mobile robots. In addition to robotic application, ultrasonic sensors are used in many other applications in different fields such as echography in medical field, non-destructive testing of materials, Advantages that encourage us to use ultrasonic sensors is the ease to obtain distance information from immediate objects without intensive processing which can considerably lighten the application. They are also able to perform under low visibility conditions making it ideal for night as well as day use. Thus, ultrasound sensor seems to be a good solution for our system to detect and recognize several objects. However, object recognition under different viewing conditions is still a challenge for autonomous systems. So, the motivation of our work is to challenge by applying only one ultrasound sensor for obstacle recognition taking into account the weaknesses of this sensor type. Many features can be extracted from the ultrasonic signal, providing different information and descriptions that are used to describe the detected object.

3. SYSTEM DESIGN

Ideally, the detected path should be shoulder width, vertical from ground level to the level of the user's head, and up to a few meters ahead of the user. Our approach is to develop an active ultrasonic device to improve the rate of relevant detection in indoor and outdoor crowded environments. Our purpose is to detect shoulder-width openings that are a long distance away (4–6 m). Our goal is to offer not only an efficient and reliable cane, but also a low cost one.
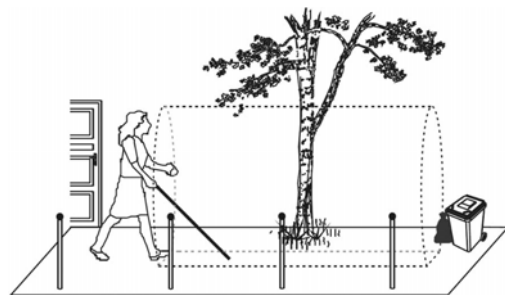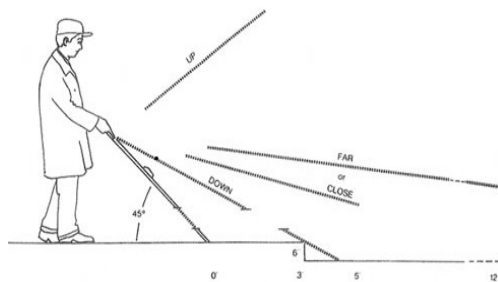

Fig 3.1 Ideal protection volume (dashed lines).

A. Sensors

1) Different sensor types

The use of different sensors is required, in different fields, to help the user in making a decision. Accordingly, we distinguish active and passive sensors. A passive sensor measures a full energy provided by a physical phenomenon. In general terms, the sensors that use external energy sources to observe an object are called passive sensors. An active sensor provides some kind of energy such as microwave, sound, light, etc., into the environment in order to detect the changes that occur on the transmitted energy. That means it transmits and detects at the same time. The most used active sensors are ultrasonic, laser, and radar. Ultrasonic sensors work well for close obstacles unlike laser ones, which operate well for distant obstacles.

2) Choice of the sensor

The choice of an active sensor depends on the measurement range of the sensor, its response time, resolution, recognition reliability and finally the application requirements. The sensors selection must take into account the area of operation of each one and its performance. Also, it depends on several factors: detection range, cost, desired precision of the measurements, type of obstacle and type of scene.

The choice of an active sensor depends on the measurement range of the sensor, its response time, resolution, recognition reliability and finally the application requirements. For this end, a comparative survey is achieved and given in Table

	Laser	**Radar**	**Ultrasound**
Principle	Transmission and reception of light wave	Transmission and reception of electromagnetic wave	Transmission and reception of ultrasonic waves
Range	About 60 meters	About 250 m	From 3 cm to 10 meters
Accuracy	High (about 5 cm)	Medium (few meters)	Very high (5 mm)
Price	Very high	high	Low

B. Electronic Components

The ATmega16 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega16 achieves through puts approaching 1 MIPS per MHz allowing the system designed to optimize power consumption versus

processing speed. The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

Fig.3.2 AVR, Vibration Motor, Ultrasonic Srf05 Sensor.

The ultracane comprises four sensors: three ultrasonic sensors and an infrared sensor. The ultrasonic sensors (srf-05) are used to detect the closest obstacle within 3.5 m in front of the user. The infrared sensor (2Y0A710) is used to detect drop-offs. A microcontroller (ATmega16) processes the sensor signals and controls the vibration motors (DMJBRK30CU) and other electronics along with the buzzer for auditory feedback. The vibration motors encode the obstacle distance information, and the buzzer alerts the user of drop-offs. Three

switches are integrated into the system in order to turn the device on and off, and to switch between the different modes. A rechargeable lithium-ion battery is used to power the electronics. Light emitting diodes (LEDs) were used to visualize the sensor values, and a Bluetooth module was integrated to wirelessly stream sensor data to a PC for development and evaluation purposes.

C. Prototype Design

The long stick is the most popular navigational aid for the blind. It is relatively easy to use, light and not expensive. Initially, the PVC pipes of the different sizes along with the connectors were bought and cut to meet the requirements of the stick. The AVR board is placed inside two connectors near the handle of the stick. These connecters are held together using hinges. The speaker and three Ultrasonic sensors are mounted onto the stick with the help of a plastic case which is properly drilled to hold the speaker and sensors in the required positions.

In this project, a white Polyvinyl Chloride (PVC) pipe with length about 100 cm is used as a stick. PVC has its own advantages to make it a very suitable material to be used as the walking stick compared too other material like wood and aluminum. The main strong points are:

 • Good compromise impact / rigidity.
 • Good weathering (experience of more than 40 years).
 • Very low maintenance.
 • High thermal and acoustical insulation.
 • High dimensional stability.
 • Good Fire resistance.
 • Good surface aspect with wide range of colours and appearances.
 • No moisture absorption.
 • Very good chemical resistance.
 • Possibility to be welded.

The components are placed in the PVC pipe and a separated handle is made for the user to hold the walking stick. The length of the stick is different for different person depending on the

height of the user. The ergonomic factor is important to ensure that the user is comfortable to use the walking stick. Figure 3.8 below illustrates the PVC pipe used as the walking stick.

Fig.3.1 Prototype Design of Ultrasonic Smart Cane

4. Conclusion

The conventional walking stick is limited in range because the stick only detects the object when the stick taps the object or ground. A walking stick with a distance sensor can help them to avoid the obstacles better without tapping the object or ground. Sharp infrared distance sensor is consumed to detect the object within the distance range of 10 cm to 80 cm because it is small in size and very efficient in detecting the object. A buzzer is employed as the signalling element which generates sound when the object is sensed by the IR distance sensor. As the object is getting closer to the IR distance sensor, the sound produced is becoming louder. The sound of buzzer is depending on the output voltage of IR distance sensor by varying the distance between object and the sensor.

The data taken from the experiment show that the output voltage of IR and Ultrasonic distance sensor is decreasing when the distance between object and IR and Ultrasonic distance sensor is increasing which in turn the sound volume of the buzzer is also decreasing. In conclusion, the objective of this project is

successfully achieved because a walking stick for the visually challenged using infrared distance sensor is successfully created to detect the object in front of the user within the specific distance range which can help them in mobility.

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ROBUST MEDICAL IMAGE MULTIPLE WATERMARK USING 4-LEVEL DWT

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Abstract— In this paper we propose a novel approach for medical image security during their transmission over the network. Medical images like CT, MRI, X-ray contain the patients' vital and confidential information. During transmission over network, it may face different attacks. To prevent such mishaps, embedding of watermark technique is used. In the proposed method, we propose to embed multiple watermarks in the input image for more security and robustness. The method first extracts the detected feature points from the input image by Weber law descriptors (WLD) to insert the watermarks in the optimal location in the input image. Then after insertion of watermarks, the watermarked image is transmitted over network and then at the receiving end, the multiple watermarks are extracted. The robustness of the algorithm is checked by the weighted peak signal to noise ratio (WPSNR) calculation and the efficiency is checked by normalized correlation NC calculation.
Index Terms—Medical image, Multiple watermark, DWT, Weber.

I. INTRODUCTION

Recently because of huge advancement in technologies like internet, telecommunication, we are moving towards digital era. Digital information is easy to handle, easy to store and it also provides ease of transfer and manipulation. Because of these advantages it also becomes the subject of interest in medical image applications.

Generally the medical images include patients' personal information. The patients' information is stored digitally in database. The information should be kept very securely so that only authorized person can see the information. During transfer of this information over the public network there are always some chances of attacks, forgery etc. So, now- a-days security of medical images has become huge area of interest among researchers. This is the need of time to secure the transfer of all the medical information through electronic media without any change in the medical image. We can secure this information by using techniques such as cryptography, authentication, etc. There is one more powerful method by which we can add low level signal into these images. This low level signal is known as watermark. This low level signal provides the better security without changing the original information of the image and it can be extracted from image easily. The process of adding low level signal information in digital image is called digital image watermarking. The watermark can be of any type like image, logos, audio or video. The watermarking technique is better over the cryptography technique because in cryptography after the encryption, the resultant image may not be properly visible also at the time of retrieval the information of the host image is lost which is not the problem in watermarking. In watermarking, we can add more than one watermark at a time. This process of adding more

than one watermark into the image is called multiple watermarking.

Giakaumaki et al.[1] proposed the method of embedding the multiple watermark into the image by using wavelet transform. This method used 4-level discrete wavelet transform and performed result on ultrasound image. In this technique, the capacity issue is not taken into account and just main focus is on robustness. The doctors' identification code is added in the 4th level. Index watermark is embedded into 3rd level. The method embeds the caption of patients' information in the second level. Even if it gives better integrity and security to the image, there are chances to improve image quality by increasing peak signal to noise ratio (PSNR).

Wakatani[2] presented the watermarking technique by which embedding of watermark is done in region of non interest of image. The technique used is embedded zero tree wavelet (EZW). The disadvantage of this method is that the embedded information can be extracted easily.

Hyung-Kyo Lee[3] proposed the method of watermarking by which the watermark is added in region of non interest of image .The separated region of interest itself used as a watermark .The method is used to prevent the illegal forgery. The disadvantage of this method is the value of similarity measurement between inserted watermark and extracted watermark which is called normalized correlation (NC) values are very less as compared to our method.

II. PROPOSED METHOD

A. Algorithm

In this algorithm for medical image security multiple watermarks are embedded in the medical images, where, depending upon the quantization of selected coefficients, multiple watermarks embedding procedure is used.

Image acquisition:

The first step is image acquisition. The medical image in which the watermark is to be embedded is first acquired from the user and then resized to a fixed size. This image is then converted to grayscale image for further processing and then assigned as reference image.

Four level Haar decomposition:

According to working domain, watermark can be applied in spatial domain or frequency domain. In spatial domain the watermark is added directly in the host data. Though it is simple method of addition of watermark, it is less robust. Watermark can be removed easily by applying some basic operations. So, we are moving towards the frequency domain. Some famous transform domains are DFT, DCT and DWT. The DFT gives the information about the frequency and amplitude. But in some applications like Synthetic aperture RADAR, there is need of time information also. Because of this reason the DWT becomes the most suitable transform among the researchers as it gives the frequency, amplitude information along with information of at which time the signal is applied. The DWT converts the image from spatial domain to frequency domain. The wavelet stands for an orthogonal basis of vector space.

When we apply 2D-DWT on the image, the image is divided into four levels LL, LH, HL and HH. The level LL contain low frequency information, it is the level where most of the image information is stored. The level LH contain the medium frequency information, it is the level where horizontal detail of image is stored. The next level i.e. HL contain the vertical detail. Final level HH contain the high frequency information of image. Further you can increase the level by using decomposition of the low frequency band.
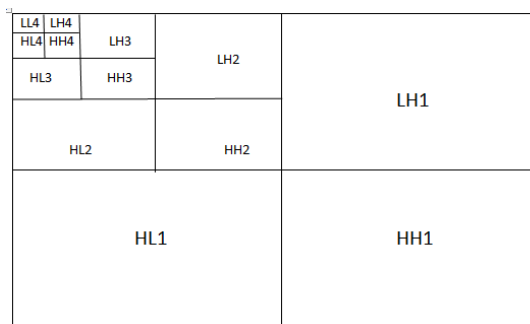

Fig. 1

Haar Wavelet Transform:

Haar wavelet is discontinuous and it resembles the unit step function. This property is advantageous for analysis of signal with sudden transition. It can be represented mathematically

as follows:

$$\psi(x) = \begin{cases} 1 & x \in [0,0.5) \\ -1 & x \in [0.5,1] \\ 0 & x \in [0.5,1] \end{cases}$$

and

$$\psi_i^j(x) = \sqrt{2^j}\psi(2^j x - i)$$

(1)

Haar is the difference and averaging phenomenon of neighboring pixels. This can be explained by following example. We took 1-D image with 8 pixels.

[4 3 -2 -3 4 1 5 1]

By applying the Haar wavelet on this image we get two types of coefficient i.e. transformed coefficient and detailed coefficient. The transformed coefficient is obtained by taking the average of two consecutive pixels. The detailed coefficient can be obtained by taking the difference of two consecutive pixels at a time and dividing the difference by 2. The detailed coefficient is used for the reconstruction of image. So, after applying one time Haar wavelet transform, the obtained image is:

Transformed coefficient= [3.5 -2.5 2.5 3]
Detailed coefficient= [0.5 0.5 1.5 2]

Feature Point Detection using Weber Local Descriptor:

For feature point detection from the reference image at level 3 and level 4 in H3 and H4 coefficients of the Haar DWT Weber local descriptor [6] is used. The Weber's law states that the ratio of increment threshold and the original stimulus intensity remains constant. The increment threshold represents the just noticeable difference. To extract the feature points from the reference image we calculate the two WLD components i.e. differential excitation (ε) and orientation (θ). First step is to calculate the differential excitation ε. Considering the 3 x 3 mask as shown in Fig. 2 (a), the value of the center pixel is subtracted from the value of each of its neighbor as shown below in Fig. 2 (b). This difference gives us the increment threshold mentioned in the Weber's law. The original stimulus intensity is nothing but the value of the center pixel considered in the above 3 x 3 mask. The original pixel intensity value can be obtained by applying another 3 x 3 mask as shown below in Fig. 2 (c).

(a)Input image   (b) mask 1   (c) mask 2
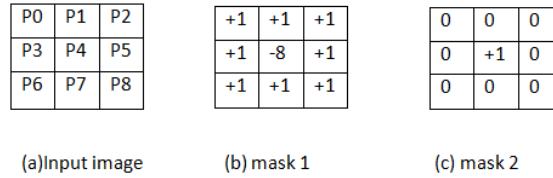
Fig. 2

According to the Weber's law, the ratio of the difference between the neighboring and center pixel to the original pixel intensity is constant. The difference between the center and neighboring pixels is calculated by following formula:

$$v1 = \sum_{k=0}^{n-1}(P_k - P_4)$$

(2)

The difference image obtained after applying mask 2 is referred as V2. And the ratio V1/V2 is constant. Then the arctangent function is employed to this ratio to compute the differential excitation ε. Thus the differential excitation is calculated by the following formula:

$$\varepsilon(P_4) = arctan\left[\frac{V1}{V2}\right] = arctan\left[\sum_{k=0}^{n-1}\left(\frac{P_k - P_4}{P_4}\right)\right]$$

(3)

Because of the delimitation property of arctangent function to limit the output even though the input fluctuates, the arctangent function is used here.

The next step is to calculate orientation (θ). To calculate the orientation value two different masks are used as shown below in the Fig. 3.

(a)Input image   (b) mask 3   (c) mask 4

Fig. 3

The masks are represented by the following formulae:

$$V3 = (P_7 - P_1) \quad and \quad V4 = (P_3 - P_5)$$

(4)

Then by using these masks, the orientation θ is calculated as

$$\theta(P_4) = arctan\left(\frac{V4}{V3}\right)$$

(5)

The value of this θ falls in the range of [-∏/2, ∏/2]. So the θ is mapped θ' into range [0, 2∏]] by using following formulae:
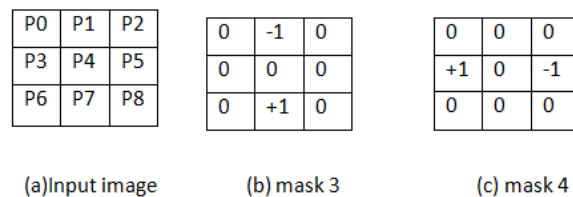
$$\theta' = arctan2(V4, V3) + \prod$$

$$arctan2(V4, V3)$$
$$= \begin{cases} \theta & V4 > 0 \ and \ V3 > 0 \\ \Pi - \theta & V4 > 0 \ and \ V3 < 0 \\ \theta - \Pi & V4 < 0 \ and \ V3 < 0 \\ -\theta & V4 < 0 \ and \ V3 > 0 \end{cases}$$

(6)

Thus by applying the WLD mask to input image, we scan the entire image. The scanning is done in such a way that the mask overlaps the next columns and rows of the input image so that the high intensity feature points are extracted from the input image, thus making the algorithm more robust and efficient. While extracting the feature points from the input image, the no. of feature points are counted so as to calculate the size of the watermark to be inserted. The feature points extracted from the image are from the 3rd and 4th level of the Haar DWT. The locations of the pixels from where the feature points are extracted are saved for insertion of watermark.

Watermark Image Resizing:
The next step after feature point extraction is the watermark resizing. As mentioned above, the scanning is done by overlapping the mask across entire image. Thus the no. of feature points extracted from the input image are in large range of numbers. The watermark image size is decided depending upon these no. of features extracted. To resize the watermark image, the square root of the no. of feature points is taken. The single-level two-dimensional wavelet decomposition with respect to a particular wavelet decomposition filters, low pass or high pass of the watermark image is then computed. The DWT of watermark image is computed for robustness. DWT gives better results than DCT. If we add watermark in low frequency band, then there are chances of loss of data and if we add the watermark in high frequency band, then the process of recovery of watermark becomes tedious. So the watermark is embedded in the medium frequency band. The watermark image is then resized by the square root of the no. of feature points extracted, after applying DWT.

Watermark insertion:
In the pixel locations from where the feature points are extracted, the resized watermark is embedded. As the method proposed here is based on multiple watermarks, two separate watermarks are embedded into the input medical image, by same method explained above. The two watermarks are embedded in the 3rd and 4th level for security and robustness. The watermark can consist of the patient's information, doctor's information, fingerprint or the image of patient or any other logo. In this method, we have embedded patient's and doctor's information as watermark images. After insertion of watermark, before sending the watermarked image on the network, the Inverse DWT of the watermarked image is taken for security purpose. After watermark insertion, single-level two-dimensional wavelet reconstruction with respect to the low pass and high pass filter is performed.

Insertion of reference watermark in Image:
In our proposed method, for checking the robustness of the system, a reference watermark is embedded into the input image. As mentioned earlier, the watermark can be inserted in both spatial and frequency domain. The reference watermark is inserted in the spatial domain to check the efficiency of the system to attacks. The insertion of watermark in spatial domain is more prone to attacks than that of frequency domain. The reference watermark is embedded into the input image by XOR operation on the bits of the watermark image.

Calculation of WPSNR:
The weighted peak signal to noise ratio (WPSNR) [5] is the image quality metric. It is an extension of peak signal to noise ratio (PSNR). WPSNR is especially useful where geometric distortions are observed, in our case, the attacks like rotation, scaling may cause the geometric distortions in the input image. The difference between PSNR and WPSNR is the Noise Visibility Function (NVF) which is included in WPSNR. The NVF enables us to know the best location in the input image for embedding watermark and its strength for embedding process. PSNR does not take into account the flat

and textured regions of the image so WPSNR is more advantageous than PSNR. So we have calculated WPSNR value of the watermarked image. The results are mentioned in the result section. Following is the formula used for calculation of WPSNR:

$$WPSNR = 10 \log_{10} \left(\frac{Maximum\ Pixel\ value}{\sqrt{MSE} \times NVF} \right)^2$$

(7)

Where MSE is mean square error which is calculated as follows:

$$MSE = \frac{1}{xy} \sum_{m=0}^{x-1} \sum_{n=0}^{y-1} \|img(m, n) - img\_v(m, n)\|^2$$

(8)

And NVF is calculated by following formula:

$$NVF(m, n) = \frac{1}{1 + \theta. \sigma_x^2(m, n)}$$

(9)

Where $\sigma_x^2(m, n)$ represents the local difference between the neighbouring pixels and θ controls the value of NVF. The value of θ is dependent on the image variance as given by following formula:

$$\theta = \frac{D}{\sigma_{Maximum}^2(m, n)}$$

(10)

Recovery of watermark:
At the receiving end, the reference watermark is recovered to check the effect of attacks. The procedure for the recovery of reference watermark is as explained in this section. First the watermarked image is XORed with the input image as we are working in spatial domain. Then the 4-level DWT is applied on the watermarked image for recovery of the reference watermark. The extraction process is exactly reverse of that of the insertion of the watermark. Again in the received image, for the extraction of other two watermarks, the WLD is used to find out the feature points in 3rd and 4th level. By using these feature points and the size of the watermark image, the watermark is recovered from the received image. This recovered watermark is then resized by the size of square-root of the no. of feature points extracted. The inverse DWT is

applied to the resized watermark image. As the proposed method consists of multiple watermarks, the same procedure is applied twice for the two different watermark extraction processes.

Calculation of Normalized correlation (NC):
The NC computes the similarity measurement between the original watermark and the extracted watermark. NC is calculated for both the watermarks. The computed values of NC for the medical images are tabulated in the results section. The formula used for computation of NC is given as follows:

$$NC = \frac{\sum_{x=1}^{N} \sum_{y=1}^{N} w(x, y) * w'(x, y)}{\sum_{x=1}^{N} \sum_{y=1}^{N} w(x, y)^2}$$

(11)

where w(x,y) represent the original and w'(x,y) represent the recovered watermark.

III. EXPERIMENTS AND RESULTS

The proposed method is applied on different types of medical images like CT scan images, MRI, X-ray and ultrasound images. The images are taken from http://www.nlm.nih.gov/research/visible.

We have tested our algorithm on medical images of size

CT scan images 512 x 512
MRI images 512 x 512
X-ray images   416 x 596
Ultrasound   358 x 256

A. Experiments and results without attack:

The algorithm was tested on the above images and the resulting images for the experiments without attack are as shown below:

CT

MRI

X-ray

Ultrasound
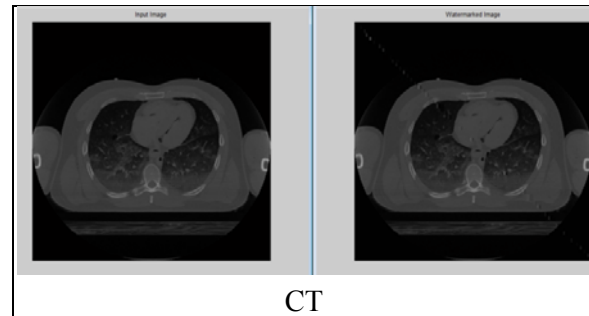
Fig. 4

The following table shows the values of WPSNR and NC for all the medical images without attack:

Types of images	WPSNR	NC for watermark1	NC for watermark 2
CT Scan	69.34 db	0.9875	0.9986
MRI	51.97 db	0.9903	0.9988
X-Ray	58.63 db	0.9908	0.9986
Ultrasound	55.27 db	0.9925	0.9989

Table 1

B. Experiments and results without attack:

The following attacks were added to the input medical images:

1. Median Filtering attack
2. Noise:

- Speckle Noise
- Poisson Noise
3. Rotation attack
4. Translation attack

The results after adding attacks were as follows:

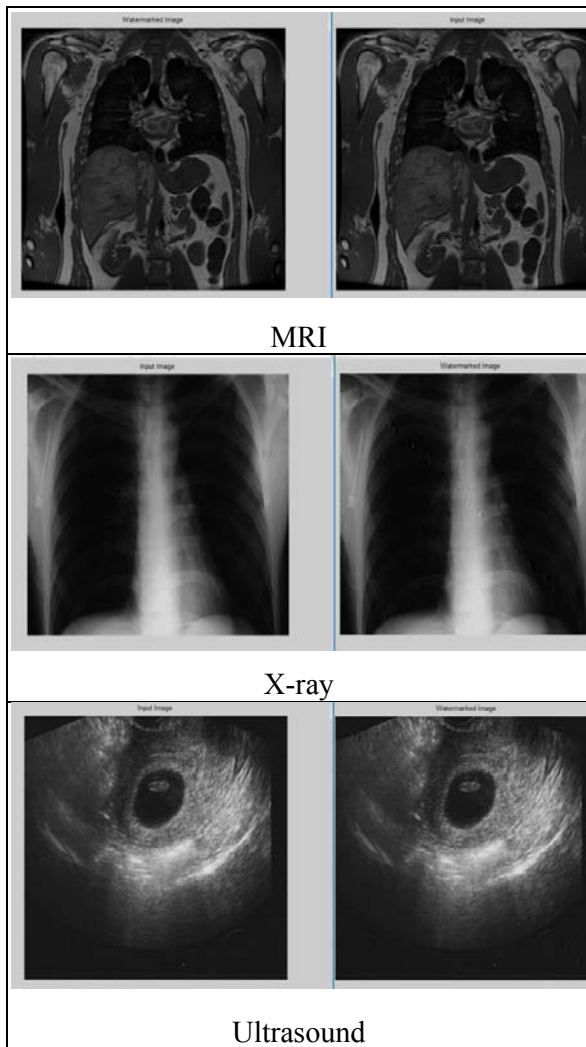| Types of attacks	WPSNR	NC for watermark1	NC for watermark 2
Median Filtering	63.70 dB	0.9884	0.9987
Speckle Noise	53.00 dB	0.9879	0.9985
Poisson Noise	47.03 dB	0.9914	0.9985
Rotation attack	54.73 dB	0.9882	0.9987
Translation Attack	39.20 dB	0.9978	0.9988

Table 2

IV. CONCLUSION AND FUTURE WORK

For the security of medical images over network, there are many methods proposed. The proposed system makes use of embedding of multiple watermarks. The system embeds the watermark using WLD and DWT method. Use of WLD and DWT makes the system robust and efficient to attacks. The results i.e. the values of WPSNR and NC show the robustness of the system. For the future work, the combination of DCT and DWT can be used to make the system more robust.

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DISCONTINUOUS PWM TECHNIQUES FOR OPEN-END WINDING INDUCTION MOTOR DRIVE FOR ZERO SEQUENCE VOLTAGE ELIMINATION

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Abstract— In now a days modern multi level inverters have emerged to overcome the drawbacks due to the conventional inverters. In various industries inverters with different PWM techniques have been employed to achieve good performance in the context of variable speed drives. But in the conventional inverter instantaneous sum of all the phase voltages is not equal to zero this results into zero sequence voltages in inverters. This zero sequence voltages will induce bearing currents inside the motor. If these currents exceed some permissible limits premature failure of motor bearings will occur. These are some drawbacks due to the usage of conventional inverters in industries. In this paper the techniques to overcome the drawbacks due to conventional inverter have been presented. The cascaded connection of asynchronous motor and two 2-level inverters at both ends of motor constitutes to open end winding induction motor drive. The characteristics of dual inverter fed open end winding induction motor drive resembles to those of conventional three level inverter . In this paper the performance characteristics of Induction motor with different PWM techniques like SPWM, CSVPWM,DPWMMAX, DPWMMIN have been analysed and the harmonic analysis has been carried out using MATLAB/SIMULINK environment.

Index Terms— Bearing currents, zero sequence voltage, CSVPWM, Open end winding induction motor drive Modulation index.

I. INTRODUCTION

Conventional two level inverters are extensively used in medium voltage and high power variable speed drive systems because of their inherent switching operation but however have some limitations in operating at high frequency mainly due to switching losses and constraints of device rating. These switching converters can also provokes high dv/dt caused due to the switching transients[1-2]. These zero sequence voltages results into various adverse effects on motors named as bearing currents, conducted electromagnetic interference, ground currents through stray capacitors. In consequence to this premature motor bearing failures will occur. The clear indication of flowing of hazardous bearing currents in the context of motors inside the motors can be shown in the Fig.1.

capacitive current coupled to the rotor
capacitively coupled from the stator winding to the rotor
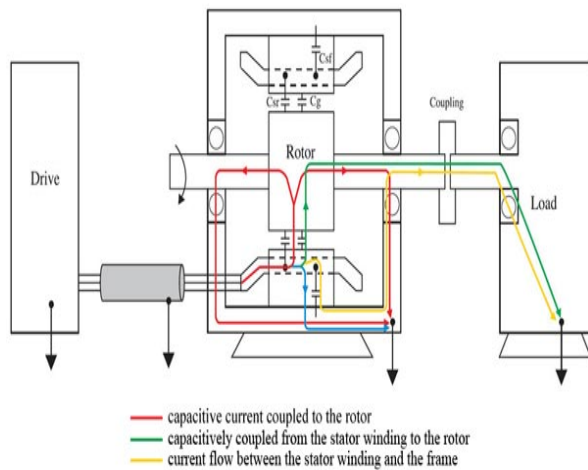current flow between the stator winding and the frame

Fig.1 Flow of bearing currents inside the motor
So concerning to this the hazardous common mode voltages in the context of variable speed motors has to be mitigated [4,10].

The numerous methods for mitigating common mode voltage in inverters can be classified as[4]:
[A].Using isolation transformers, Common mode choke, Using hybrid active and passive filters, Using dual inverter fed open end winding induction motor drive, Using four phase inverter.
[B].Using some advanced modulation techniques like carrier based SVPWM scheme for dual inverter fed open end winding IM drive.

The methods proposed in [A] above increases the system cost as it employs some extra hardware circuitiry and complexity in control. So this is mainly focused on the implementation of SVPWM technique for dual inverter fed open end winding induction motor. A schematic of dual inverter fed open end winding induction motor can be represented as shown in the Fig.2.
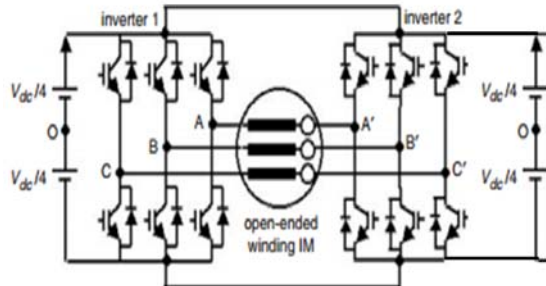

Fig.2 Dual inverter fed open end winding Induction motor drive

As dual inverter fed open end winding induction motor drive resembles the performance of three level inverter thus we can achieve multilevel inverter operation using this configuration. Hence the harmonic content of the output voltage waveform decreases significantly, dv/dt stresses are reduced, Produces smaller zero sequence voltages therefore stress in the bearings of motor can be reduced, Provides low switching losses and higher efficiency[5-8].

II.SPWM(SINUSOIDAL PULSE WIDTH MODULATION TECHNIQUE)

The sinusoidal pulse width modulation technique produces a sinusoidal waveform by filtering an output pulse waveform with varying width. A high switching frequency assures a better filtered sinusoidal output waveform. The desired output voltage is achieved by varying the frequency and amplitude of a reference or modulating voltage i.e. by varying the modulation index. The variations in the amplitude and frequency of the reference voltage can change the pulse width pattern of the output voltage.

The gate pulses to the inverter switches generated by comparing a low frequency sinusoidal modulating waveform with a high frequency triangular waveform [11]. The switching state is changed when the sine waveform intersects the triangular waveform. The crossing positions determine the variable switching times between states.

In three phase inverter for switching of devices of the inverter, a triangular wave is compared with three sinusoidal voltages which are 120^0 out of phase with each other.

The relative levels of the waveforms are used to control the switching of the devices in each leg of the inverter. The sinusoidal pulse width modulation technique can be well explained with the comparison of triangular wave & modulating (sinusoidal) wave as shown in the Fig.3

The modulation ratio(ρ) is the ration between frequency of carrier wave to that of the modulating wave i.e. reference wave & is represented by the eqn(1).
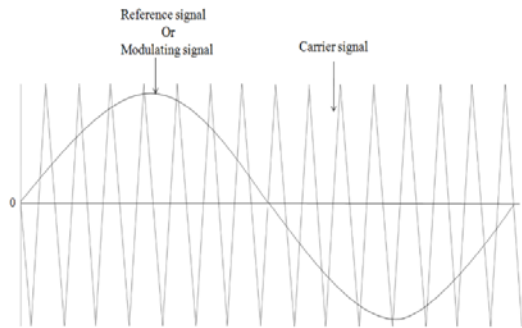
$$\rho = \frac{fc}{fm} \qquad (1)$$

Fig.3 Carrier and reference wave comparison for SPWM control technique

The modulation index(M) is the ratio between the amplitude of modulating wave to that of the carrier wave & is represented by eqn(2).

$$M = \frac{Am}{Ac} \qquad (2)$$

The modulation ratio (ρ) is related to harmonic frequency as

$$f = k \, \rho \, f_m \qquad (3)$$

Generally the magnitude of modulation index is limited below one(i.e. 0<m<1)

Drawbacks due to SPWM:
1. Precise & flexible control of voltage is not possible.
2. Generates more Harmonic distortion in output.
3. DC bus utilization is not that much effective.

To overcome these drawbacks due to conventional SPWM control technique an advanced control technique is proposed known as Space Vector Pulse Width Modulation Technique.

III.SVPWM CONTROL TECHNIQUE

SVPWM control technique is an advanced modulation technique abbreviated as Space Vector Pulse Width Modulation Technique has several advantages over other pulse width modulation techniques like superior performance in terms of better harmonic spectra, ease of implementation and advanced & enhanced dc bus utilization[12].The concept of SVPWM technique

can be well explained with the help of a rotating voltage vector as shown in the Fig.4.
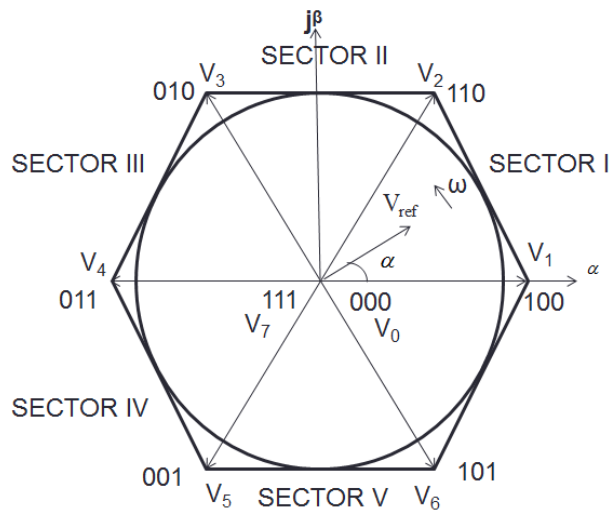
Fig.4 SPACE VECTOR

1).Principle of Space vector:

A typical two level inverter has 6 power switches (S_1 to S_6) that generates three phase voltages. The six switching power device can be constructed using power BJTs, GTOs, IGBTs the choice of switching devices is based on the desired operating power level, required switching frequency & acceptable invertible power losses. When the upper transistor is switched on, the corresponding lower transistor is switched off. The on & off states of lower power devices are complementary to the upper power devices.

The basic principle of SVPWM is based on the eight switching combinations of three phase inverter. The eight(8) switching combinations of a three phase inverter can be represented in the Table.1.

S.NO.	Switching State	ON state devices
1	000	4,6,2
2	100	1,6,2
3	110	1,3,2
4	010	4,3,2
5	011	4,3,5
6	001	4,6,5
7	101	1,6,5
8	111	1,3,5

Table.1:Switching states and ON State Power devices

The switching combinations are represented in binary form. In this '1' indicates the on state of upper switching device in the corresponding phase leg & '0' indicates the on state of lower device in the corresponding phase leg.

The instantaneous sum of all the phase voltages is calculated & they deduce six(6) active vectors and two(2) zero vectors lies on the diagonals of hexagon. And the two zero vectors lies at the centre of the hexagon.

The reference vector which represents the 3φ sinusoidal voltages can be synthesised using SVPWM by switching between two nearest active vectors & zero vectors. The switching of reference vector with active and zero vectors can be represented as shown in the fig(5).
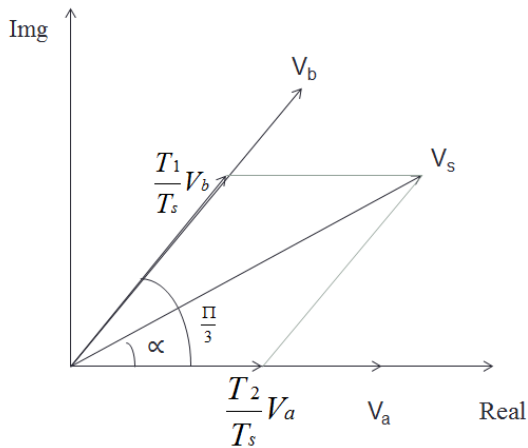

Fig.5 Synthesizing of reference vector from active and zero vectors

The time of application of these vectors can be calculated by volt second balancing as

$$\int_0^{T_z} V_{ref} = \int_0^{T_1} V_1 \, dt + \int_0^{T_1+T_2} V_2 \, dt + \int_{T_1+T_2}^{T_z} V_2 \, dt \quad (4)$$

By solving the above equation we get

$$T_z V_{ref} = T_1 V_1 + T_2 V_2 \quad (5)$$

$$T_1 = 3 \frac{V_{ref}}{V_{dc}} \left[\frac{\sin(60-\alpha)}{\sin(60)} \right] * T_s$$

$$T_2 = 3 \frac{V_{ref}}{2V_{dc}} \left[\frac{\sin(\alpha)}{\sin(60)} \right] * T_s \quad \Bigg\}$$

$$T_0 = T_z - (T_1 + T_2) \quad (6)$$

Where V_{ref}= reference voltage vector magnitude

α = is the angle or position of the reference vector

T_1, T_2, $T_{0=}$ are the time of application of vector V_1,

vector V_2, zero vector V_0 respectively.

2)CSVPWM(Continuous Space Vector Pulse Width Modulation Technique):

In all PWM algorithms SVPWM gives good performance in terms of harmonics & effective control but the complexity is more due to angle calculations & sector identification. To reduce this complexity carrier based SVPWM algorithm is developed by adding offset voltage to the reference phase voltage. The switching pattern for the three phases using carrier based SVPWM can be represented as shown in theFig.6.
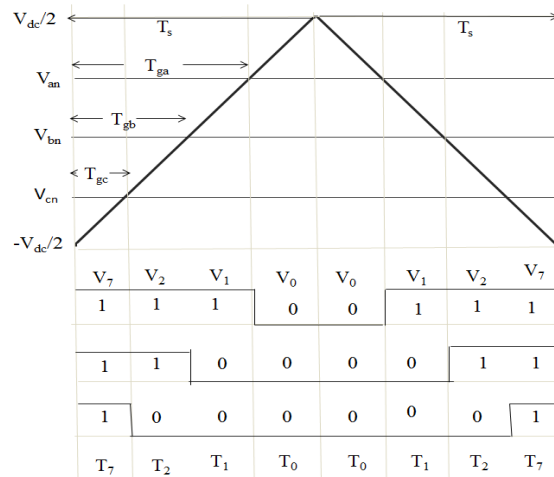
Fig.6 Switching pattern of power devices using carrier based SVPWM control technique

In order to achieve fixed switching frequency & optimum harmonic performance from SVPWM each branch should change its state only once in one switching period. This is achieved by applying zero vector followed by two adjacent active vectors in half switching period is the mirror image of the first half. The total switching period is thus divided into 7 parts. The zero vector is applied for 1/4th of the total zero vector time first. Followed by the application of active vectors for the half of their application times & then again zero vector is applied for 1/4th of the zero time. This is then repeated for the next half switching period.. This is how the symmetrical CSVPWM is achieved.

3) Discontinuous PWM technique(DPWM):

The main feature of space vector PWM is the freedom of explicit pulse placement in half of the carrier cycle. By using this degree of freedom alternative space vector PWM strategy can be formulated in which the active vectors in two successive half switching period are moved to join together, and zero space vector consequently vanishes resulting in Discontinuous Space vector PWM (Houdsworth and Grant, 1984). Due to this manipulation one branch of the inverter remain unmodulated during one switching interval. Switching takes place in two branches and one branch is either tied to the positive dc bus or negative dc bus. The number of switching is thus reduced to 2/3 compared to the continuous SVPWM, hence, the switching losses are reduced significantly. Six different schemes are available depending on the variation in the placement of the zero space vectors.

1. $T_0 = 0$ (DPWMMAX)
2. $T_7 = 0$ (DPWMMIN)
3. 0^0 Discontinuous modulation (DPWM 0)
4. 30^0 Discontinuous modulation (DPWM 1)
5. 60^0 Discontinuous modulation (DPWM 2)
6. 90^0 Discontinuous modulation (DPWM 3)

4) Zero sequence voltage elimination scheme with Open end winding configuration:

A remedy for the production of flowing of bearing currents inside the motors is open end winding induction motor. In this configuration Induction motor is feeded by two inverters from either side which are operated be isolated power supplies. A schematic diagram of dual inverter fed induction motor is represented as shown in Fig.7.
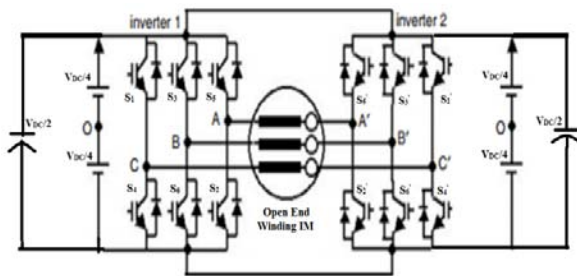

Fig.7 Dual inverter fed open end winding IM drive

Here $S_1, S_2, S_3, S_4, S_5, S_6$ are the switches of inverter 1 and $S_1', S_2', S_3', S_4', S_5', S_6'$ are the switches of inverter 2. The two inverters are supplied with isolated DC links, If the isolated DC link voltages are equal(i.e.$V_{s1}=V_{DC}/2$ &

$V_{s2}=V_{DC}/2$) then the configuration resembles to that of three level inverter drive. If the Isolated DC link voltages are unequal (i.e. $V_{s1}=2V_{DC}/3$ & $V_{s2}=V_{DC}/3$) then the configuration resembles to that of four level inverter. In this 1& 0 represents on states of switches of inverter 1, $1'$ & $0'$ represents on states of switches of inverter2 .

Here V_{A0}, V_{B0}, V_{C0} are the pole voltages of inverter 1, $V_{A0}', V_{B0}', V_{C0}'$ are the pole voltages of inverter 2.$V_{AA}', V_{BB}', V_{CC}'$ are the Phase voltages of the inverter which are supplied to the three phase induction motor but here the sum of all these phase voltages is not equal to

$$CMV \text{ or } V_{ZS} = \frac{V_{AA}' + V_{BB}' + V_{CC}'}{3}$$

zero, which results as zero sequence component in motor due this the bearing currents will flow inside the motor . But here carrier based SVPWM algorithm is proposed to mitigate this Common mode voltage. The three phase voltages of dual inverter fed induction motor drive is given by

$$V_{AA}' = V_{A0} - V_{A0}'$$
$$V_{BB}' = V_{B0} - V_{B0}'$$
$$V_{CC}' = V_{C0} - V_{C0}' \qquad (7)$$

Where V_{A0}, V_{B0}, V_{C0} are the pole voltages of inverter 1,

$V_{A0}', V_{B0}', V_{C0}'$ are the pole voltages of inverter 2

$\& V_{AA}', V_{BB}', V_{CC}'$ are the Phase voltages of the inverter

The common mode voltage or Zero sequence voltage is given by

$$CMV \text{ or } V_{ZS} = \frac{V_{AA}' + V_{BB}' + V_{CC}'}{3} \qquad (8)$$

The reference voltage in SVPWM modulation technique will be obtained as represented in equation (4)

$$V_{ref} = V_{AA}' + V_{BB}' e^{j2\pi/3} + V_{CC}' e^{j4\pi/3} \qquad (9)$$

Hence by employing this open end winding configuration multilevel inverter operation can be achieved and the problems due to conventional inverters like common mode voltages can be overcome.

IV.SIMULATION RESULTS

A) For single inverter Fed IM drive with SPWM control:

A two level inverter fed induction motor drive is modelled and is simulated by employing sinusoidal pulse width modulation(SPWM) control technique and the carrier and triangular comparison waveform, output pole, phase voltages of the inverter are shown in Fig.8
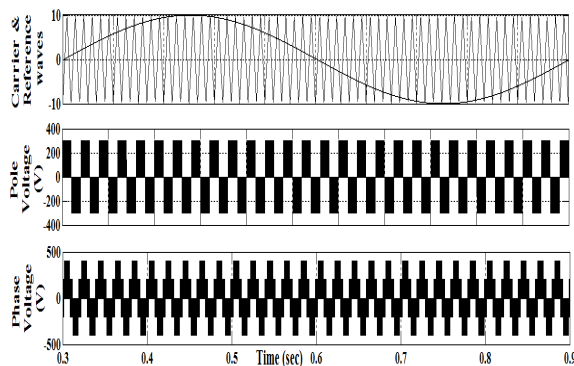

Fig.8 Carrier and reference wave comparison, Pole Voltage, Phase voltage of single inverter with SPWM

The performance characteristics of Induction motor drive i.e. Stator currents, Torque response, Speed response with no load and with the application of load of 20Nm at 0.5sec up to 0.7sec are as shown in Fig.9 and Fig.10 respectively .The motor achieves steady state at 0.3 sec. with the application of load at 0.5 sec the stator currents, Torque of the motor increases in proportion to load but the speed decreases in proportion to the load and after removal of load at 0.7 sec the motor comes to steady state position .
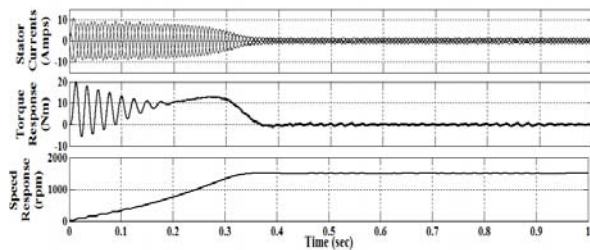
Fig.9 Performance characteristics of IM drive with single inverter(SPWM) at no load
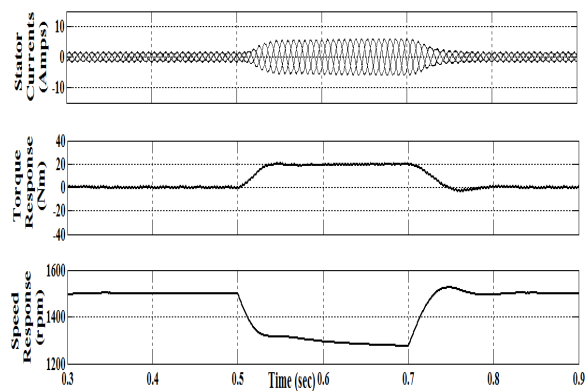
Fig.10 Performance characteristics of IM drive with single inverter(SPWM) under load condition with T_L=20Nm

B)For single inverter Fed IM drive with SVPWM control:

A two level inverter fed induction motor drive is modelled and is simulated by employing space vector pulse width modulation(SVPWM) control technique and the Modulated waveform, output pole, phase voltages and the common mode voltage of the inverter are shown in Fig.11

Fig.11 Modulated wave, Pole voltage, Phase Voltage, CMV for Single inverter with SVPWM

The performance characteristics of Induction motor drive i.e. Stator currents, Torque response, Speed response at no load and with the application of load of 20Nm at 0.5sec upto 0.7sec are as shown in Fig.12 and Fig.13 respectively. The motor achieves steady state at 0.3 sec. with the application of load at 0.5 sec the stator currents, Torque of the motor increases in proportion to load but the speed decreases in proportion to the load and after

removal of load at 0.7 sec the motor comes to steady state position and the Total Harmonic Distortion(THD) for the stator currents is 7.26% for this model.
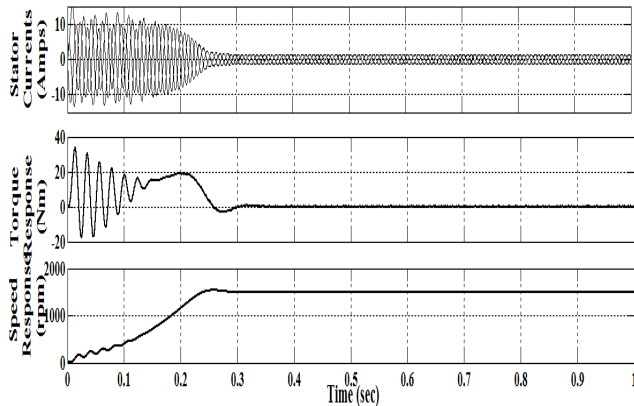
Fig.12 Performance characteristics of IM drive with single inverter(SVPWM) at no load
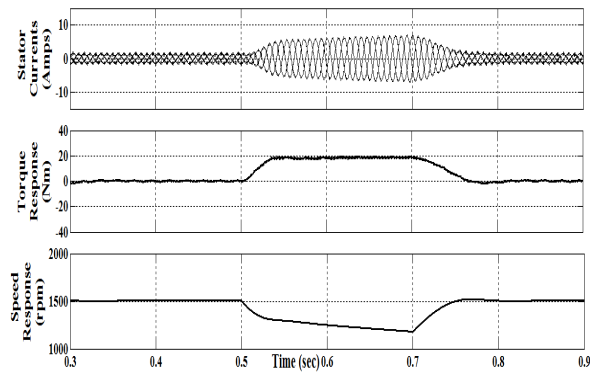
Fig.13 Performance characteristics of IM drive with single inverter(SVPWM) under load condition with T_L=20Nm

B)For dual inverter Fed IM drive(three level inverter operation) with CSVPWM, DPWMMAX,DPWMMIN control

A dual inverter fed induction motor drive is modelled and is simulated by employing space vector pulse width modulation(CSVPWM) control technique and the Modulated waveform, output pole, phase voltages and the common mode voltage of the inverter which resembles the characteristics of three level inverter characteristics are shown in Fig.14

Fig.14Modulating Wave, Pole voltage, Phase Voltage, Common mode voltage for dual inverter (Three level inverter operation)with CSVPWM control technique

The performance characteristics of Induction motor drive i.e. Stator currents, Torque response, Speed response at no load and with the application of load of 20Nm at 0.5sec upto 0.7sec are as shown in Fig.15 & Fig.16 respectively. The motor achieves steady state at 0.25 sec. with the application of load at 0.5 sec the stator currents, Torque of the motor increases in proportion to load but the speed decreases in proportion to the load and after removal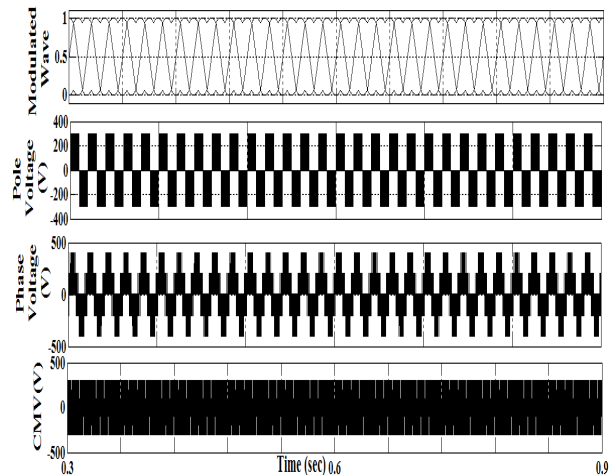 of load at 0.7 sec the motor comes to steady state position and the Total Harmonic Distortion(THD) for the stator currents is 4.77% for this model & the common mode voltage is mitigated compared to single inverter fed IM drive.

Fig.15 Performance characteristics of dual inverter (Three level inverter operation(CSVPWM))fed IM drive at no load

Fig.16 Performance characteristics of dual inverter (Three level inverter operation(CSVPWM))fed IM drive under load condition with T_L=20Nm

A dual inverter fed induction motor drive is modelled and is simulated by employing space vector pulse width modulation(DPWMMAX)control technique and the Modulated waveform, output pole, phase voltages and the common mode voltage of the inverter which resembles the characteristics of three level inverter characteristics are shown in Fig.17

Fig.17 Modulating Wave, Pole voltage, Phase Voltage, common mode voltage for dual inverter (Three level inverter operation)with DPWMMAX control technique

The performance characteristics of of dual inverter fed Induction motor drive(three level inverter operation)with DPWMMAX control i.e. Stator currents, Torque response, Speed response at no load and with the application of load of 20Nm at 0.5sec upto 0.7sec are as shown in Fig.18 & Fig.19 respectively. The motor achieves steady state at 0.25 sec. with the application of load at 0.5 sec the stator currents, Torque of the motor increases in proportion to load but the speed decreases in proportion to the load and after removal of load at 0.7 sec the motor comes to steady state position

and the Total Harmonic Distorsion(THD) for the stator currents is 3.97% for this model & the common mode voltage is mitigated compared to single inverter fed IM drive.

Fig.18 Performance characteristics of dual inverter (Three level inverter operation with DPWMMAX)fed IM drive at no load

Fig.19 Performance characteristics of dual inverter (Three level inverter operation with DPWMMAX)fed IM drive under load condition with T_L=20Nm

A dual inverter fed induction motor drive is modelled and is simulated by employing space vector pulse width modulation(DPWMMIN)control technique and the Modulated waveform, output pole, phase voltages and the common mode voltage of the inverter which resembles the characteristics of three level inverter characteristics are shown in Fig.20
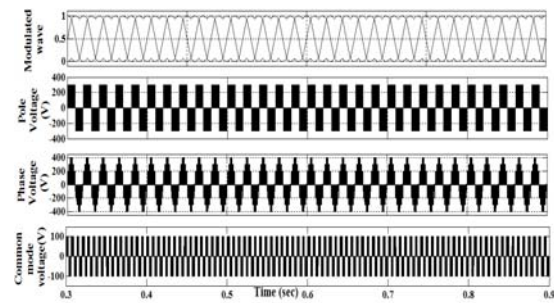
Fig.20 Modulating Wave, Pole voltage, Phase Voltage, common mode voltage for dual inverter (Three level inverter operation)with DPWMMIN control technique

The performance characteristics of of dual inverter fed Induction motor drive(three level inverter operation)with DPWMMIN control i.e. Stator currents, Torque response, Speed response at no load and with the application of load of 20Nm at 0.5sec upto 0.7sec are as shown in Fig.21 & Fig.22 respectively. The motor achieves steady state at 0.25 sec. with the application of load at 0.5 sec the stator currents, Torque of the motor increases in proportion to load but the speed decreases in proportion to the load and after removal of load at 0.7 sec .the motor comes to steady state position and the Total Harmonic Distortion (THD) for the stator currents is 3.85% for this model & the common mode voltage is mitigated compared to single inverter fed IM
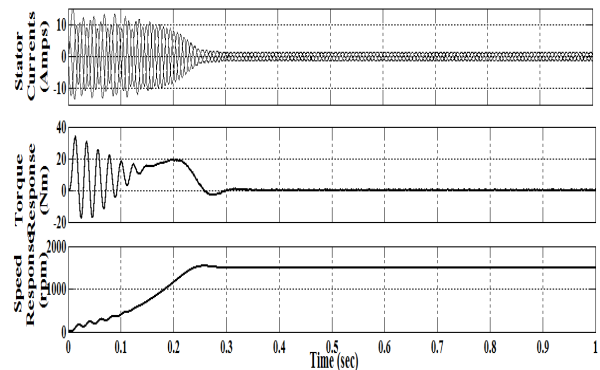

drive.

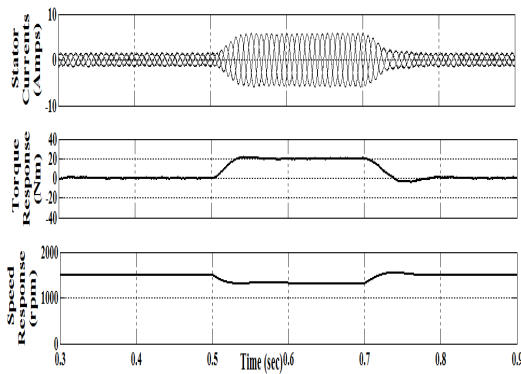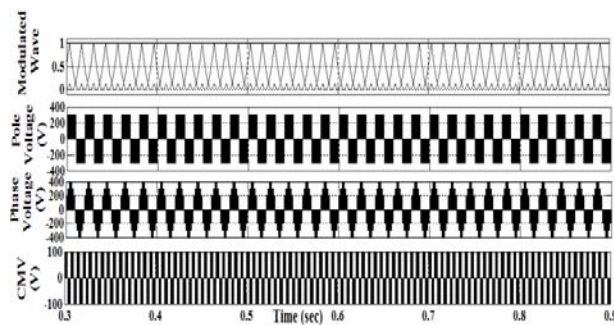Fig.21 Performance characteristics of dual inverter (Three level inverter operation with DPWMMIN control) fed IM drive at no load

Fig.22 Performance characteristics of dual inverter (Three level inverter operation with DPWMMIN control) fed IM drive under load condition with T_L=20Nm

C)For dual inverter Fed IM drive(Four level inverter operation)with CSVPWM, DPWMMAX,DPWMMIN control

A dual inverter fed induction motor drive is modelled and is simulated by employing space vector pulse width modulation(CSVPWM) control technique and the Modulated waveform, output pole, phase voltages and the common mode voltage of the inverter which resembles the characteristics of four level inverter characteristics are as shown in Fig.23

Fig.23 Modulated wave, Pole voltage, Phase voltage, Common mode voltage for dual inverter(Four level inverter operation with CSVPWM control)

The performance characteristics of of dual inverter fed Induction motor drive(four level inverter operation)with CSVPWM control i.e. Stator currents, Torque response, Speed response at no load and with the application of load of 20Nm

at 0.5sec upto 0.7sec are as shown in Fig.24 & Fig.25 respectively. The motor achieves steady state at 0.25 sec. with the application of load at 0.5 sec the stator currents, Torque of the motor increases in proportion to load but the speed decreases in proportion to the load and after removal of load at 0.7 sec the motor comes to steady state position and the Total Harmonic Distortion (THD) for the stator currents is 4.77% for this model & the common mode voltage is mitigated compared to dual inverter fed IM drive with three level inverter operation.
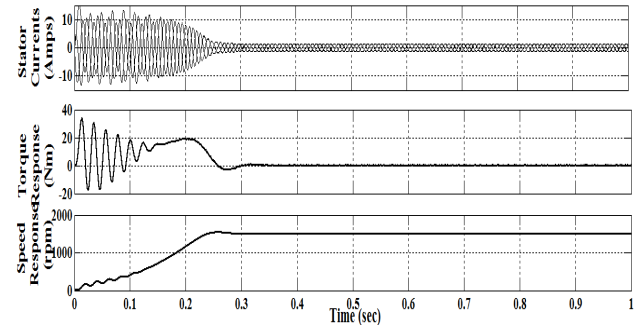
technique and the Modulated waveform, output pole, phase voltages and the common mode voltage of the inverter which resembles the characteristics of four level inverter characteristics are as shown in Fig.26

Fig.26 Modulated wave, Pole voltage, Phase voltage, Common mode voltage for dual inverter(Four level inverter operation with DPWMMAX control)

Fig.24 Performance characteristics of dual inverter
(Four level inverter operation(CSVPWM)) fed IM drive at no load

The performance characteristics of of dual inverter fed Induction motor drive(four level inverter operation)with DPWMMAX control i.e. Stator currents, Torque response, Speed response at no load and with the application of load of 20Nm at 0.5sec upto 0.7sec are as shown in Fig.27 & Fig.28 respectively. The motor achieves steady state at 0.25 sec. with the application of load at 0.5 sec the stator currents, Torque of the motor increases in proportion to load but the speed decreases in proportion to the load and after removal of load at 0.7 sec the motor comes to steady state position and the Total Harmonic Distorsion(THD) for the stator currents is 3.85% for this model & the common mode voltage is mitigated compared to dual inverter fed IM drive with three level inverter operation.

Fig.25 Performance characteristics of dual inverter
(Four level inverter operation(CSVPWM)) fed IM drive under load at TL=20Nm

A dual inverter fed induction motor drive is modelled and is simulated by employing space vector pulse width modulation(DPWMAX) control

Fig.27 Performance characteristics of dual inverter
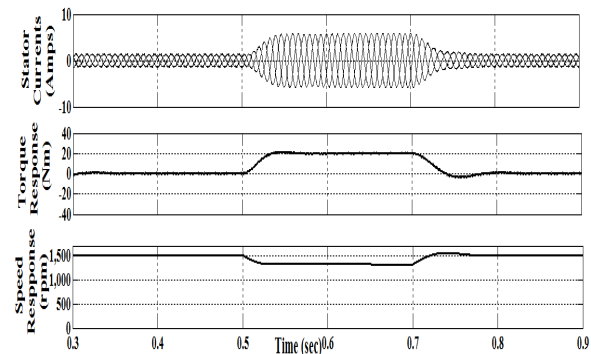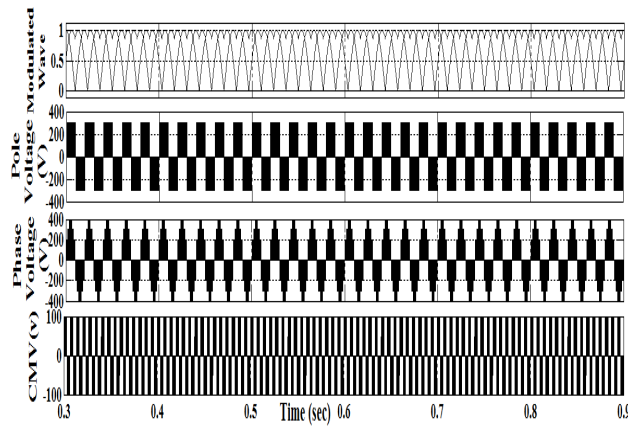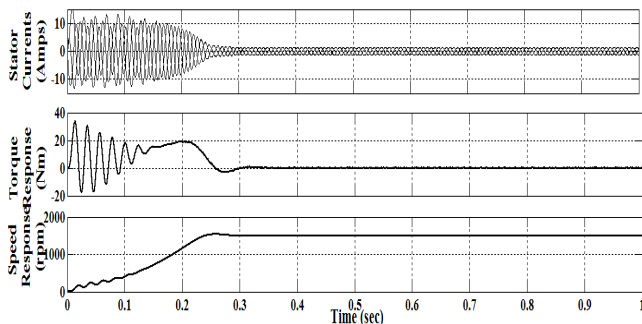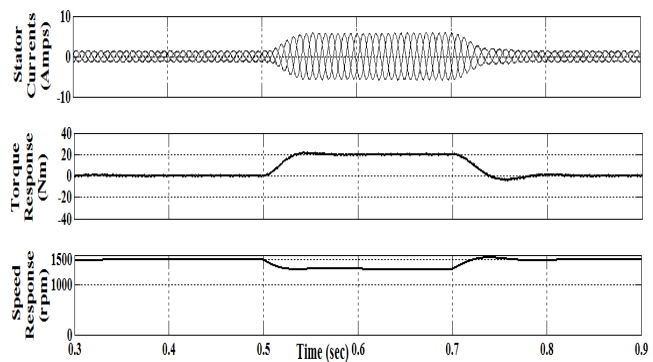(Four level inverter operation(DPWMMAX control))
fed IM drive at no load

Fig.28 Performance characteristics of dual inverter
(Four level inverter operation(DPWMMAX control))
fed IM drive under load condition with T_L=20Nm

A dual inverter fed induction motor drive is modelled and is simulated by employing space vector pulse width modulation(DPWMMIN) control technique and the Modulated waveform, output pole, phase voltages and the common mode voltage of the inverter which resembles the characteristics of four level inverter characteristics are as shown in Fig.29
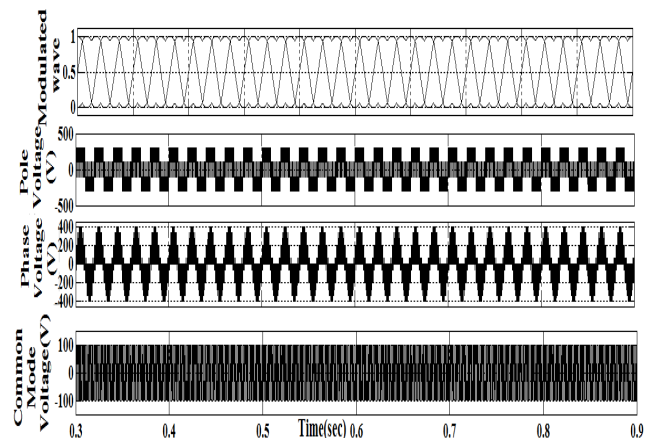

Fig.29 Modulated wave, Pole voltage, Phase voltage, Common mode voltage for dual inverter(Four level inverter operation with DPWMMIN control)

The performance characteristics of of dual inverter fed Induction motor drive(four level inverter operation)with DPWMMIN control i.e. Stator currents, Torque response, Speed response at no load and with the application of load of 20Nm at 0.5sec upto 0.7sec are as shown in Fig.30 & Fig.31 respectively. The motor achieves steady state at 0.25 sec. with the application of load at 0.5 sec the stator currents, Torque of the motor increases in proportion to load but the speed decreases in proportion to the load and after removal of load at 0.7 sec the motor comes to steady state position and the Total Harmonic Distortion(THD) for the stator currents is 3.43% for this model & the common mode voltage is mitigated compared to dual inverter fed IM drive with three level inverter operation.
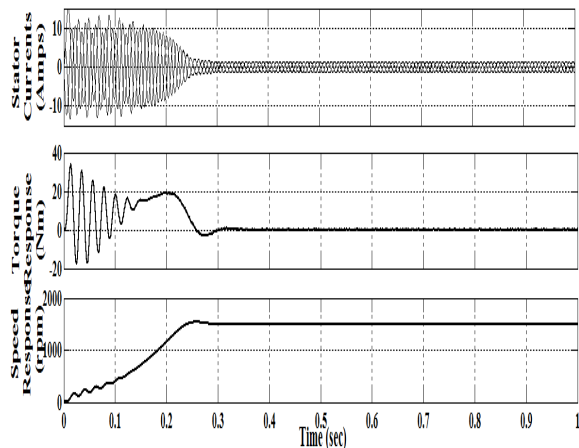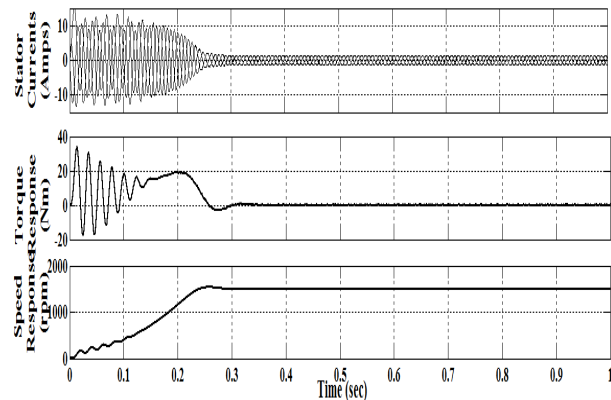

Fig.30 Performance characteristics of dual inverter
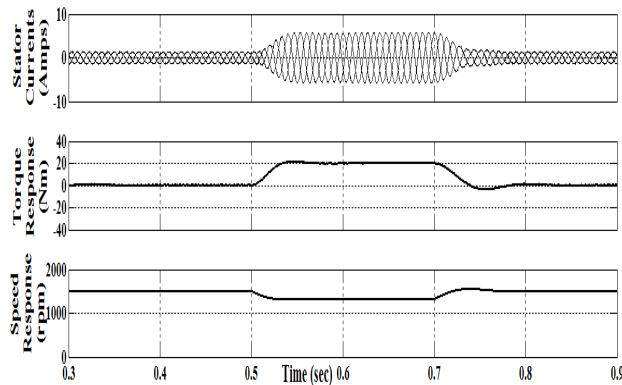(Four level inverter operation (DPWMIN control))
fed IM drive at no load

Fig.31 Performance characteristics of dual inverter
(Four level inverter operation(DPWMMIN control))
fed IM drive under load condition with
T_L=20Nm

D)THD Comparison:

The THDs for stator currents of IM drive is listed out as shown in the Table.2.

Inverter Type	Control technique	THD of stator currents of the Motor(I_{THD})
2 level	SPWM	18.28%
	SVPWM	7.26%
3 level	CSVPWM	4.77%
	DPWMMAX	3.97%
	DPWMMIN	3.85%
4 level	CSVPWM	4.51%
	DPWMMAX	3.85%
	DPWMMIN	3.43%

Table.2 Comparison of stator currents THDs for various control techniques

IV.CONCLUSION

In this paper the implementation of dual inverter fed induction motor drive has been done. With the implementation of triangular based SVPWM the machine performance will be improved in the context of harmonic spectra and effective DC bus utilization over the conventional sinusoidal pulse width modulation technique. And the zero sequence voltage problem is also mitigated at a greater level compared to other mitigating techniques. This work can be extended with the

implementation of SVPWM for higher level(5,6,7 levels) for dual inverter fed open end winding induction motor.

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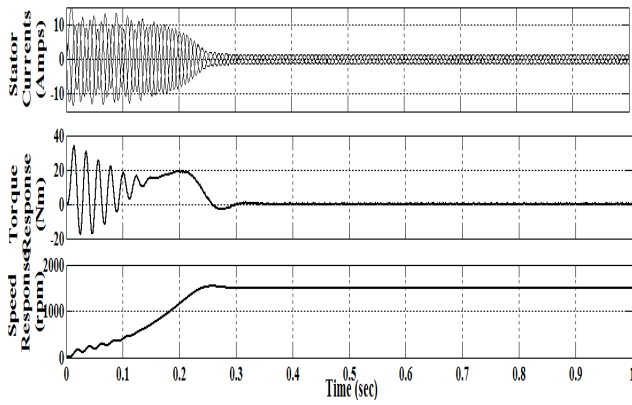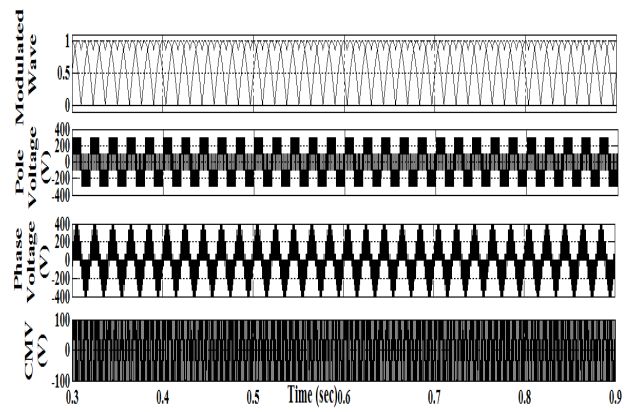
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WIRELESS SENSOR NETWORK BASED INTELLIGENT HOME IMPLEMENTING USING ARDUINO AND ZIGBEE

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Abstract— **Automation and security is a one of the important issue in a modern domestic environment. This system focus on developmental and research issues of Wireless Sensor Network based Smart Home. Wireless Sensor Network based smart home monitoring system provides a secure and safe living environment. A Wireless Sensor Network (WSN) is a network which is constructing by using small autonomous nodes (sensors). Its purpose is to monitor certain environmental parameters such as temperature, humidity, brightness, pressure, sound, motion, etc.**

This system describes the development of a smart home environment based on accurate Wireless Sensor Network using Zigbee and also describes residential energy monitoring and controlling techniques for smart home networking system. This paper propose a simple and flexible wireless network for domestics automation of temperature, humidity, gas, motion and light by implementing reliable sensor nodes which can be controlled as well monitored. This technology offers exciting and new opportunity to increase the connectivity of devices within the home for the home automation.

Keywords—Home automation, Wireless sensor network, Arduino and Zigbee

I. INTRODUCTION

In developing world everyone feel happier in a comfortable and secure home environment.

Constructing an intelligent and safe home environment is one of the important and most attractive issues for many researchers and engineers. Several industries and research have attempted to construct intelligent environment by installing intelligent sensors and devices. To provides services for user all these sensors, devices are integrated by wireless network [2].

Integration of smart devices as well smart network in residential area can be making it smart and also helpful to manage energy appropriately, effectively. Such a smart home provides various advantages with Wireless Sensor Network includes remote monitoring, continuous data recovery, energy consumption, location tracking, management of temperature and humidity, motion detection, understanding and observation of the people's environment [12].
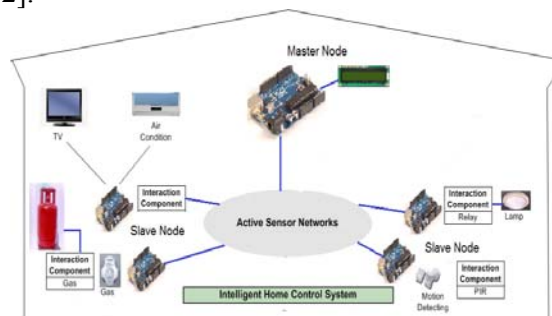

Fig. 1 Intelligent Home Control System

Smart home system is an intelligent home network together with advanced communication technology and sensing control technology to carry out effective control and information exchange [10]. WSN are gradually being used in the home for energy management services likes

lighting is automatically controlled through information such as the resident's movement or the intensity of illumination gathered by WSN and consumer devices are monitored and controlled by WSN installed in the home [1].

The Home Automation system provides mutual interoperability among the different electronics and electrical devices. This system also provides interactive interface for people to control their operation and this will very helpful to optimize and economize energy consumption [8]. Home automation is upcoming trends that people looks for residential houses, apartments, commercial uses. People want to live in more intelligent living spaces to make their life easier, safer and more enjoyable [9].

Zigbee based wireless sensor network is used as a new short range wireless communication technology which is low data rate, low power consumption, highly reliable, fast reaction, programmable, robustness and security [2]. Zigbee is a local area network designed specifically for application of automation or control system [8]. Zigbee is a best solution for WSN which is based on IEEE 802.15.4 standard and is extended with network and application for upper layers for simplifying the design effort of a WSN application. With proper integration of Zigbee and sensors it would be efficient to develop and build wireless real time monitor and control system [11].

II. REQUIREMENTS OF A HOME AUTOMATION SYSTEM

A Home Automation System fulfils the following requirements in order to improve existing conditions of environment. Home Automation is applied to a wide range of products and systems in the home likes refrigerator, washing machine, dishwasher, oven, vacuum cleaner, home theatre, DVD, television, night lights, electricity, security against fire, gas leaks, water leaks, electrical leakage and short circuit, assistance to disabled person, elderly and children, domestic environmental monitoring, energy consumption monitoring, health monitoring, etc.

1. Comfort: The system needs all the tools to simplify and make easier the liveability within the home. It ensures that the level of perceived occupant comfort is as high as possible which includes ease of use of the various Home Automation System functions.

2. Energy saving: In this all the techniques and systems capable to optimize energy consumption which able to source the cheapest energy source.

3. Safety: System is intended as protection from possible malfunction of equipment potentially dangerous or harmful to people and housing which are used fire protection systems, anti-flooding, different sensors like gas, smoke etc., loads of power transmission.

4. Security: Security is the control of the access from the outside like burglar alarms and access control systems, computer attacks, since they are coming from the external network, are managed by several technologies such as Proxy, Firewall.

5. Stability: Stability is a system ability to react to failures of individual modules in order to avoid mistakes that could compromise the functioning of the entire automated environment [4].

III. WIRELESS SENSOR NETWORK

Recent advances in sensing, computing and communication technologies coupled with the need to continuously monitor physical phenomena have led to the introduction of Wireless Sensor Networks (WSNs). Wireless sensor networks (WSNs) are special kind of ad-hoc and dynamic wireless network which consists of number of wireless sensor nodes. Each sensor node is capable of limited amount of processing and power. But when they are coordinated with other nodes in the network, they have the ability to communicate over the large range.

WSNs are an emerging technology that is being used to collect information for various environmental parameters such as temperature, pressure, illumination of light, humidity etc. WSNs are has a variety of application domains e. g. home, office, automation and control, transportation, logistics, healthcare, environmental monitoring, security and surveillance, process monitoring, vehicle monitoring and detection and it also have concerns about energy-efficiency, security, reliability and scalability, habitat monitoring, and disaster detection, vehicular traffic management, precision agriculture.

WSN consist of four major components: A radio, a processor, sensors and battery. The key constraints for development of WSNs are

limited battery power, cost, limited computational capability, and the physical size of the sensor nodes. Wireless sensor networks have features like Reliability, Accuracy, Flexibility, Cost efficiency, Ease of Installation. Most commonly used wireless communications standard in WSNs is based on the IEEE 802.15.4, known as Zigbee.

A recent issue regarding WSNs is that it is one of the top 10 emerging technologies according to IEEE spectrum. WSNs may either connect to the various cellular networks or through the wired internet. A sensor network provides easy access for the information from anywhere at every time. This should be achieved by collecting; processing, analysing and spreading data thus wireless sensor network plays an important role in creating smart environments.
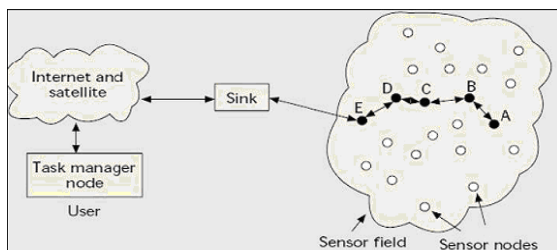
Fig. 1 Wireless Sensor Network architecture

The typical wireless sensor network consists of following fields:

Sensor Field*:* A sensor field is nothing but the area in which the nodes are placed.

Sensor Nodes*:* Sensors nodes are the heart of the network, they are in charge of collecting data and routing this information back to a sink.

Base Station*:* It is a centralized point of control within the network, which extracts information from the network and disseminates control information back into the network, also serves as a gateway to other networks. It is a powerful data processing and storage center and an access point for a human interface also. The base station is nothing but a workstation.

User: User is the controller or a person who want the information of wireless sensor network to take decision [13].

IV. ARDUINO

The fundamental unit of Wireless Sensor Network is a Sensor Node, also called as mote. Each sensor node is required to be capable of sensing, processing and communicating the

processed data to the neighbouring nodes to form a network. Sensor node is hence composed of sensors to sense the physical phenomenon, analog to digital converter, microcontroller for controlling and data processing, memory for algorithms and data storage, radio unit for short range wireless communication and battery unit to power all the units.

Fig. 2 Wireless Sensor Network node - Arduino

Arduino is a tool for making computers that can sense and control more of the physical world than your desktop computer. It's an open-source physical-computing platform based on a simple microcontroller board, and a development environment. Arduino can be used to develop interactive objects, taking inputs from a variety of switches or sensors, and controlling a variety of lights, motors, and other physical outputs. The Arduino programming language is an implementation of Wiring, a similar physical-computing platform, which is based on the Processing multimedia-programming environment.

The Arduino Uno is a microcontroller board based on the ATmega328. It has 14 digital input/output pins (of which 6 can be used as PWM outputs), 6 analog inputs, a 16 MHz crystal oscillator, a USB connection, a power jack, an ICSP header, and a reset button. It contains everything needed to support the microcontroller; simply connect it to a computer with a USB cable or power it with an AC-to-DC adapter or battery to get started. The Uno differs from all preceding boards in that it does not use the FTDI USB-to-serial driver chip. Instead, it features the Atmega8U2 programmed as a USB-to-serial converter [ ].

V. ZIGBEE OVERVIEW

ZigBee is a wireless communication technology for short coverage, low data rate, less complication, low power and low cost. It's widely used in the field of auto-control and

remote control. ZigBee is based on IEEE802.15.4 standard and it co-ordinates thousands of tiny sensors. These sensors send the data from one sensor to another through radio waves and consequently provide high telecommunication efficiency. In brief, ZigBee is a low cost, low power, short coverage wireless network communication technology compare with the other existing technology such as WiFi, Bluetooth, IR, etc.

Table 1.Comparision of Wireless technology

Features	Wi-Fi	Bluetooth	ZigBee
Battery Life Time	Several hours	Several days	Several years
Complexity	High	Complex	Simple
Nodes Number	32	7	65,000
Communication time	3 seconds	10 seconds	30 milliseconds
Coverage	100m	10m	10m-several Km
Data Rate	11 Mbps	1 Mbps	250 Kbps

A. *Zigbee network architecture*

In general, a complete ZigBee network contains 3 major parts: ZigBee Coordinator, ZigBee Router and End Device.

- ZigBee Coordinator: The coordinator is the central unit of a Zigbee network. The generation of network beacon, controlling the formation of network topology and coordinating the communication and flow rate of the devices in the network.

Fig. 3 Zigbee network architecture

- ZigBee Router: The transmission of data, coordination of flow rate of some devices in the network, sending and receiving commands and data, and permitting subsidiary device comes under the supervision of router. It also helps to extend the coverage of ZigBee network that's why it is also called as repeater.

- End Device: End device present at the bottom of network topology, which supervise sending and receiving data and execute commands. Generally, there should not be hand over data to other devices [3].

VI. SYSTEM ARCHITECTURE
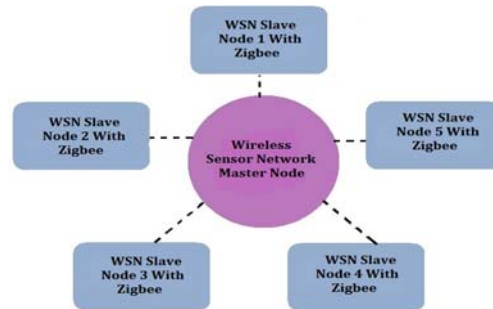
Fig. 4 system architecture

System architecture consists of one master node and several slave nodes which are connected wirelessly in a network. The sensor node includes Arduino uno board, Zigbee module and different sensors like temperature, light, gas, humidity and PIR sensor. These sensors are interface with the Arduino board. The detail of sensor node will be in next section.

A. *WSN node with its components*

A sensor node, also known as a mote in a wireless sensor network that is capable of performing processing, gathering sensory information and communicating with master or other connected nodes in the network. A mote is a node but an every node is not always a mote.
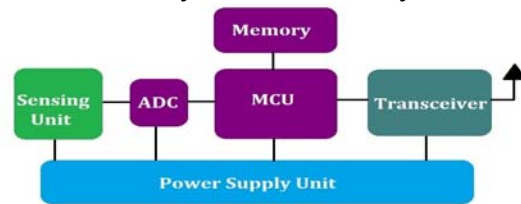
Fig. 5 sensor node

A sensor node generally consists of following major parts:

- Computation: It consists of a microcontroller (MCU) which is responsible for the control of the sensors and execution of communication protocols. The controller performs tasks, processes data and controls the functionality of other components in the sensor node. MCU's usually operate under various operating modes for

power management. Shuttling between these operating modes involves consumption of power, so the energy consumption levels of the various modes should be considered for the battery lifetime of each node.

- Communication: The possible choices of wireless transmission media are radio frequency (RF), optical communication (laser) and infrared communication. Radio frequency-based communication is generally fits for most of the WSN applications. WSNs tend to use license-free communication frequencies like 173, 433, 868, and 915 MHz; and 2.4 GHz. The functionality of both transmitter and receiver are combined into a single device known as a transceiver which consists of a short range radio device which is used to communicate with neighboring nodes and the outside world.

- Sensing: It consists of a group of sensors. Sensors are hardware devices that produce a measurable response to a change in a physical condition like temperature or light. Sensors measure physical data of the parameter to be monitored. The continual analog signal produced by the sensors is digitized by an analog-to-digital converter and sent to controllers for further processing.

- Power Supply: It consists of a battery or external supply of power to its corresponding node. Usually the rated current capacity of a battery being used for a sensor node is lesser than the minimum energy consumption required leading to the lower battery lifetimes which can be increased by reducing the current drastically or even turning it off often.[6]

B. *Structure of proposed system*
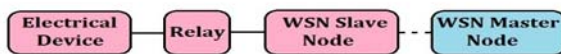
Fig. 6 General structure of proposed system

In proposed system different electrical appliances or devices can be controlled by WSN master node through WSN slave node. The communication between master node and electrical devices can be performed by Zigbee transceiver which is a wireless communication device located at WSN nodes.

Any electrical appliances such as light, FAN or AC, T.V. etc can be controlled depending upon the reference point stored in the memory of master node which is useful for decision of performance of electrical appliances e.g. if light intensity is set to 20 luminous. If illumination of light intensity goes below 20 then sensor will detect that change in intensity of light. This information is transmitted to WSN master node. Information is collected from number of WSN slave node connected to light through relay. Every slave node connected to master node by using Zigbee transceiver. According to reference point stored at master node it will take action to turn ON the light.

In the system the different sensors are used which is placed according to star topology. Each slave node connected to the required electrical appliances or devices needs to be control. The sensors will detect its corresponding physical parameter convert it into electrical signal. The converted signal will transmit the information to the WSN master node from WSN slave node. After getting the information mater node will check it with reference value of parameter and pass controlling information towards corresponding slave node to take the necessary action and through relay the electrical appliance can be operated. Likewise all the different electrical devices can be control through the automation and minimize the energy consumption.

VII. CONCLUSIONS

This paper focused on development of wireless sensor node and coordinator for intelligent home system based on Zigbee technology. We address a new intelligent home control system based on sensor networks to make home networks more intelligent and automatic. We suggest new ubiquitous home scenarios based on this proposed system. The proposed system is flexible and easy to implement sensor network having low cost, low power more reliable. An intelligent home control system can provide both significant cost savings in a home environment, as well as a great level of flexibility and control for the building administrators and great comfort for the occupants. This work focused on the

smartening of home through automation with wireless sensors working in network to continuously monitoring and controlling of different electrical devices.

ACKNOWLEDGMENT

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DESIGN OF EFFICIENT ROUTING ALGORITHM FOR CONGESTION CONTROL IN NOC

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Abstract— Congestion is an important issue in networks and significantly affects network performance. The Scheduler acts as the central switch arbiter. The fundamental component in systems which contain shared resources are arbiters and a centralized arbiter is a tightly integrated design for its input requests. In this study, we propose a new centralized arbiter, which may be used in arbitration of a crossbar switch in NoC routers. We design Islip arbiter using Islip scheduling algorithm with mesh router for NoC More integration of system component into single die are allowed increasingly by smaller feature sizes as fabrication technology continues to improve. The limiting factor for performance can be made by communication between these components unless embodying the correct scheduling algorithm.
Keywords— Network-on-Chip, System-on-Chip, On-chip routing switch, Scheduler, Islip, Synthesis

I. INTRODUCTION

In traditional System-on-Chip (SoC) design, shared buses are used for data transfer among various subsystems. As SoC design involves a larger number of subsystems, so that it becomes more complex and traditional bus-based architecture gives rise to new paradigm for on-chip communication. This paradigm is called Network-on-Chip (NoC). The most constraining aspects in the design of embedded system is the complexity, following the rapid technological evolution. The issues of cost and timing add the difficulties in realization of network-on-chip, NoC, applications, where many IPs (Intellectual Property) such as processor cores, memories, DSP processors and peripheral devices are placed together, on a single die. Most often, these modules communicate by means of a shared resource, the on-chip network. The increasing demand for higher bandwidth on the network lines, the increasing complexity of the individual devices and an operating frequency hitting new limits with almost every new design, place the communication and/or computation resources arbitration being the performance bottleneck of the NoC system. To avoid large latencies between the cores on the chip the arbitration is desired to be completed within one clock cycle (e.g., between a processing element (PE) and a memory block). The overall delay introduced by the arbitration should be low so that it will not impact the overall system clock frequency to achieve the arbitration in one clock cycle, which introduces new challenges for the design of the arbiters. The key research problems in the design of NoC include but are not limited to topology, channel width, buffer size, floor plan, routing, switching, scheduling, and IP mapping [8]. The components of the NoC include the network adapter, the routing node, and the network links [13]. The routing node in turn consists of four major components: the input ports, the scheduler,

the crossbar switch, and the output ports. Scheduling algorithms have been developed by a number of researchers [5] [6][7][8], for research prototypes [2][4], and commercial products [3]. What makes a good crossbar scheduling algorithm for the backplane of a router?

We desire algorithms with the following properties:

• High Throughput — An algorithm that keeps the backlog low in the VOQs(virtual output queuing). Ideally, the algorithm will sustain an offered load up to 100% on each input and output.

• Starvation Free — The algorithm should not allow any VOQ to be unserved indefinitely.

• Fast — To achieve the highest bandwidth switch, it is important that the scheduling algorithm does not become the performance bottleneck. The algorithm should therefore select a crossbar configuration as quickly as possible.

• Simple to implement — If the algorithm is to be fast in practice, it must be implemented in special-purpose hardware; preferably within a single chip.

Satisfying the above criterion here we present Islip arbiter using Islip scheduling algorithm with on-chip mesh router. In this study, we explore the adaptation of network techniques and methodology for addressing two particular issues in next-generation buffer less NoC design: congestion management and scalability. Buffer less NoCs have recently gained serious consideration in the architecture community due to chip area and power constraints. While the buffer less NoC has been shown to operate efficiently under moderate workloads and limited network sizes.

II. BACKGROUND

As more complex SoCs begin to emerge, the task of communication between the subsystems of an SoC cannot be adequately handled by bus based communication architectures. NoCs are proposed to be a viable alternative to bus based architectures for communication within SoCs.

A generic 2D mesh NoC architecture is shown

in figure 1.
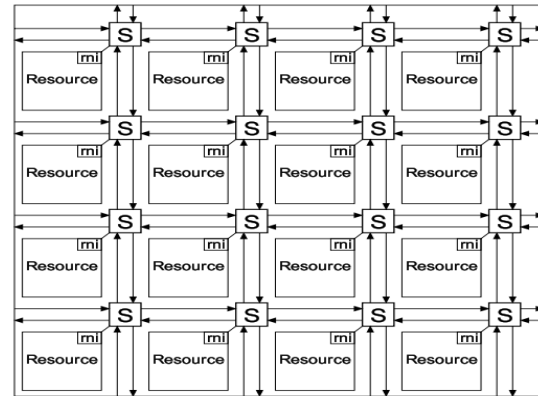
Fig. 1: SoC based on NoC

The SoC consists of a number of resources. These resources communicate with each other using an NoC. The NoC consists of the switches and point-to-point links. The internal structure of the NoC switch is given in figure 2.
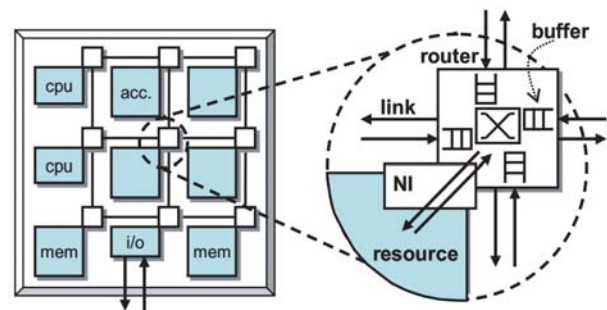
Fig. 2: NoC Switch Schematic

Each switch consists of four distinct components. A set of input blocks are connected to incoming packet lines. These input blocks contain buffers to queue the incoming packets so that they can be stored until they are ready to be transferred over the shared crossbar matrix. A set of output blocks are connected to the outgoing packet lines. No buffers are required in the output blocks as there is no possibility of conflict due to the absence of any shared resources at the outputs. The central crossbar matrix provides a direct link between each pair of input and output blocks. Finally, a scheduler is required to perform arbitration in to enable fair access to the common crossbar fabric for all incoming packets.

A. NoCs in Multi-Core Architectures:

In a chip multiprocessor (CMP) architecture,

the NoC generally connects the processor nodes and their private caches with the shared cache banks and memory controllers. A NoC might also carry other control traffic, such as interrupt requests, but it primarily exists to service cache miss requests. In this architecture, a high-speed router exists at each node, which connects the core to its neighbors by links.

B. Buffer less NoCs and Routing:

Specifically, recent work has shown that it is possible to completely eliminate buffers from the routers of on-chip networks routers. In such buffer less NoCs, application performance degrades minimally for low-to-moderate network intensity workloads, while some work shows that power consumption decreases by 20-40%, router area on die is reduced by 75%, and implementation complexity also decreases [16].

III. A GENERIC ROUND ROBIN ARBITER (RRA)
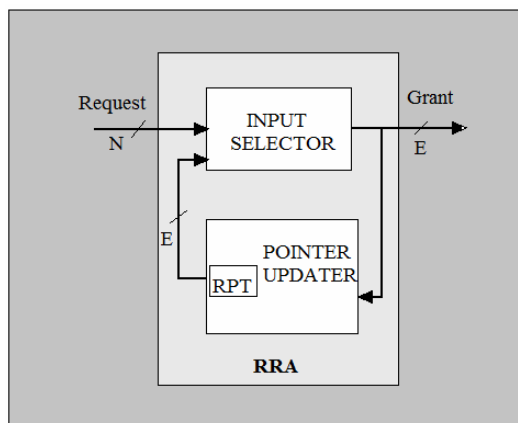
Fig. 1: Generic Round Robin Arbiter architecture

The operation of the RRA is as follows. At the beginning of every clock cycle, each input with a request sets the corresponding bit in the Request to high. Input Selector decides the input that would be granted next, based on the Request and the current value of RPT. If there is a request from the input pointed by RPT (i.e., Request [RPT] = high), this input will be granted by setting the Grant output value to the index of this input, g. If there is no request from the input pointed by RPT, but there are other requests, the

Input Selector grants the first input with a request following the pointer in a circular manner (i.e., if there is any request from inputs i > RPT, the smallest indexed input, g > RPT with a request will be granted. If there are no requests from inputs i > RPT, but there are requests from inputs, i < RPT, the smallest indexed input, g 6= RPT with a request, will be granted.). At the end of the clock cycle, the Pointer Updater sets the pointer value to the input next to the granted input in a circular manner (i.e., RPT = (g + 1) mod N). If there is no request from any inputs, the RPT will not change. An optional no request (NoReq) output port can be added to the generic RRA, which will be high when no input has a request.

I. Limitations on the Scalability of RRA:

The most time-consuming operation of the generic RRA is the granting of the requests by the Input selector, which also dominates the critical path delay. The complexity of the Input Selector is due to two main issues: (1) The issue of changing priority: The priority of the inputs changes as inputs are granted and the RPT value changes. This requires the Input Selector circuit to consider all possible priority settings. (2) The issue of circular priority order: The priority order is circular, which makes the priority processing even harder. This leads to two separate conditions for the grant decisions: Grant decisions for requests at or below the Request [RPT] and grant decisions for requests above Request [RPT]. Any grant produced by the Former decision has a higher priority over any grant produced by the latter decision. This two parted decision deepens the critical path. These two issues are even more pronounced as the RRA size gets larger (i.e., an RRA with more inputs). Also RRA has its throughput near about 63%.

IV. THE ISLIP SCHEDULING ALGORITHM

The Islip algorithm is designed to meet our goals. Islip is an iterative algorithm — during each time slot, multiple iterations are performed to select a crossbar configuration, matching inputs to outputs. The Islip algorithm uses

rotating priority ("round-robin") arbitration to schedule each active input and output in turn. The main characteristic of Islip is its simplicity; it is readily implemented in hardware and can operate at high speed. Islip attempts to quickly converge on a conflict-free match in multiple iterations, where each iteration consists of three steps. All inputs and outputs are initially unmatched and only those inputs and outputs not matched at the end of one iteration are eligible for matching in the next.

The steps for each iteration are as follows:

Step 1.: Request- Each input sends a request to every output for which it has a queued cell.

Step 2: Grant- If an output receives any requests, it chooses the one that appears next in a fixed, round-robin schedule starting from the highest priority element. The output notifies each input whether or not its request was granted.

Step 3: Accept.- If an input receives a grant, it accepts the one that appears next in a fixed, round-robin schedule starting from the highest priority element. The pointer to the highest priority element of the round-robin schedule is incremented (modulo N) to one location beyond the accepted output. The pointer to the highest priority element at the corresponding output is incremented (modulo N) to one location beyond the granted input. The pointers are only updated if and only if the grant is accepted after the first iteration. By considering only unmatched inputs and outputs, each iteration matches inputs and outputs that were not matched during earlier iterations.

V. SCHEDULAR ARCHITECTURE

The function of the scheduler is to arbitrate between requests from input blocks to output blocks. The arbitration scheme is based on a maximal size approach proposed in reference [14]. It is a variant of round robin matching, which is shown to prevent starvation under uniform traffic [14]. A scheduling decision is arrived at in three steps: (a) Requests are sent from the input blocks to the output grant generation arbiters. (b) Grant signals are generated by the output grant arbiters and sent to input accept arbiters. (c) Accept signals are

generated by the input accept arbiters and these signals represent the final scheduling decision. This decision is sent back to the input blocks as well as the crossbar switch to enable transfer of packets from the input blocks to the output blocks. The top level diagram of the scheduler is shown in figure 3.
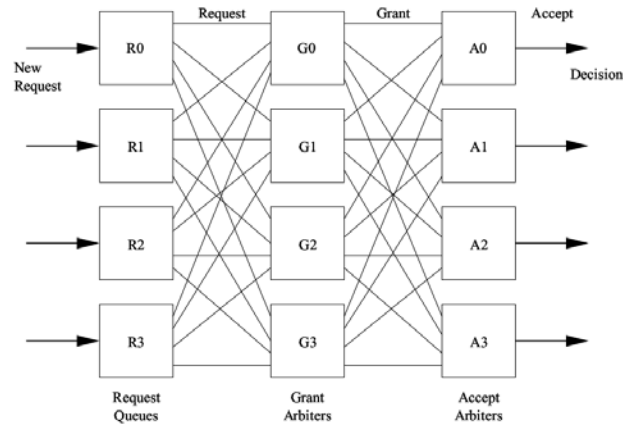
Fig 3: Scheduler Block Diagram

Each arbiter consists of a programmable priority encoder and a pointer to hold the value of the previously granted and accepted request. Figure 4 depicts the arbiter schematic.
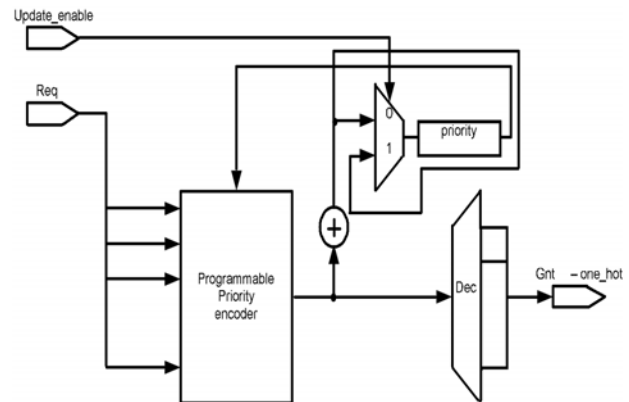
Fig 4: Arbiter Schematic

The programmable priority encoder generates a grant signal in response to a request signal based on a simple round robin scheme. Figure 5 depicts the programmable priority encoder schematic. The programmable priority encoder is realized using a hybrid design composed of two simple priority encoders. The programmable priority encoder design is based on thermometer encoding [15]. This design occupies less area compared to more classic programmable priority encoder designs. The most timing-critical

component of the scheduler design is the Programmable Priority Encoder (PPE) utilized by each Arbiter. The speed of the programmable priority encoder will determine how fast the arbitration logic can run, and is likely to be the critical paths of the overall interconnect design.

VI. IP CORE FPGA DESIGN IMPLEMENTATION METHODOLOGY

Goal: To develop a synthesizable IP core in HDL, for Islip   scheduler block of the routing logic.

A. HDL:
I. Design Description using Verilog-HDL

B. Verification Scheme:
I. Functional Simulation using Xilinx ISE Simulator
II. Test bench for top level design using Verilog-HDL
III. Stimulus for testing IP Core
IV. Simulation results / Timing diagram Analysis

C. FPGA Implementation:
I. Design to be synthesized using Xilinx ISE Software.
II. Generate a design bit stream for FPGA device.
III. Demo the download of design bit stream on FPGA device.
IV. No further verification on hardware / FPGA Kit
V. FPGA kit will NOT be provided
VI. Target Technology: Xilinx Spartan / Virtex Device.

VII. CONCLUSION

An iterative, round-robin algorithm, iSLIP can achieve 100% throughput for uniform traffic, yet is simple to implement in hardware. Prototype and commercial implementations of iSLIP exist in systems with aggregate bandwidths ranging from 50 to 500 Gb/s. When the traffic is nonuniform, iSLIP quickly adapts to a fair scheduling policy that is guaranteed never to starve an input queue. This new arbiter is fair for any input combinations and faster & it is designed using Xilinx ISE for simulation of Verilog code and Xilinx ISE for synthesis and FPGA implementation.

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PREDICTION BASED MINIMALLY BUFFERED DEFLECTION ROUTER INTERCONNECT, IN NETWORK-ON-CHIP

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Abstract— A conventional Network-on-Chip (NoC) router uses input buffers to store packets to improve performance, but consume significant power. While bufferless NoC design has shown reduction in area and power, and offers similar performance to conventional buffered designs for many workloads, than conventional buffered routers at high network load. This degradation is a significant problem for widespread adoption of bufferless NoCs.

In this work, we propose a new NOC router design called Minimally-Buffered Deflection (MinBD) Router combines deflection routing with a small buffer, which place some network traffic in this small buffer which would have been deflected otherwise. And using the prediction flow control technique for the side buffer. The side buffer would generate status signals, which are sent out to neighboring router switches, would help control the congestion in the network, by predicting the routing flow.

Key Words: Network-on-Chip, Minimally-Buffered Deflection (MinBD) Router, Prediction Buffer

I. INTRODUCTION

A network-on-chip is a component of current and future multi core and many core CMPs (Chip Multiprocessors) [10], and its design can be critical for system performance. As core counts rises, NoCs with designs such as 2Dmesh are expected to become more common to provide adequate performance scaling. Unfortunately, packet-switched NoCs are consuming significant power. In the Intel Terascale 80-core chip, 28% of chip power is consumed by the NoC [7]; for MIT RAW, 36% [35]; for the Intel 48-core SCC, 10% [3]. NoC energy efficiency is thus an important design goal [4], [5].

Bufferless yields simpler and more energy-efficient NoC designs: e.g., CHIPPER [12] reduces average network power by 54.9% in a 64-node system compared to a conventional buffered router. But, at high network traffic, deflection routing reduces performance and efficiency. This is because deflections occur more frequently when many flits contend in the network. Each deflection sends a flit further from its destination, causing unnecessary link and router traversals. Relative to a buffered network, a bufferless network with a high deflection rate wastes energy, and suffers worse congestion, because of these unproductive network hops. In contrast, a buffered router is able to hold flits (or packets) in its input buffers until the required output port is available, incurring no unnecessary hops. Thus, a buffered network can sustain higher performance at peak load. Our goal is to obtain the energy efficiency of the bufferless approach with the high performance of the buffered approach. One prior work, AFC (Adaptive Flow Control), proposes a hybrid design that switches each router between a conventional input-buffered mode and a bufferless deflection mode [8]. However,

switching to a conventional buffered design at high load incurs the energy penalty for buffering every flit: in other words, the efficiency gain over the baseline input-buffered router disappears once load rises past a threshold. AFC also requires the control logic for both forms of routing to be present at each network node, and requires power gating to turn off the input buffers and associated logic at low load. Ideally, a router would contain only a small amount of buffering, and would use this buffer space only for those flits that actually require it, rather than all flits that arrive. We propose minimally-buffered deflection routing (MinBD) as a new NoC router design that combines both bufferless and buffered paradigms in a more fine and efficient way. MinBD uses deflection routing, but also incorporates a small buffer and prediction buffer. The router always operates in a minimally-buffered deflection mode, and can buffer or deflect any given flit. When a flit first arrives, it does not enter a buffer, but travels straight to the routing logic. If two flits contend for the same output, the routing logic chooses one to deflect, as in a bufferless router. However, the router can choose to buffer up to one deflected flit per cycle rather than deflecting it. This fine-grained buffering-deflection hybrid approach significantly reduces deflection rate, and improves performance, as we show. It also incurs only a fraction of the energy cost of a conventional buffered router. Using prediction buffer and status signals, we can calculate or predict the total resource availability of the network. This information helps to avoid excess injection of packets in the network thus, reduces congestion and deflection rate. MinBD provides higher energy efficiency while also providing high performance, compared to a comprehensive set of baseline router designs.
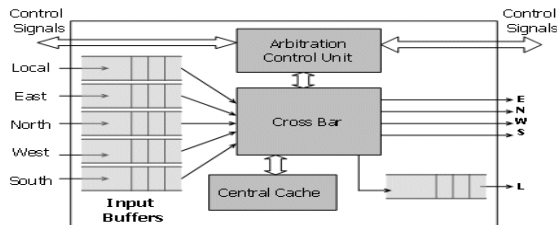
Fig. 1. Typical Router

II. BACKGROUND

On-chip networks most recently-proposed large-scale CMPs (chip multiprocessors) [3, 10, 12]. Such systems are cache-coherent shared memory multiprocessors. Interconnect has served as the substrate for large cache-coherent systems for some time, and the principles are the same in a chip multiprocessor: each core, slice of a shared cache, or memory controller is part of one "node" in the network, and network nodes exchange packets that request and respond with data in order to fulfill memory accesses. CMP NoCs are typically used to implement such a protocol between the cores, caches and memory controllers.

While many on-chip network designs have been proposed, Bufferless deflection routing was first proposed by Baran [2]. An early implementation of bufferless deflection routing for a NoC was BLESS [9], and CHIPPER [6] later provided a more efficient hardware implementation of the deflection routing and packet reassembly.

III. MOTIVATION

Previous NoC designs based on bufferless deflection routing [6], [9] were motivated largely by the observation that many NoCs in CMPs are over provisioned for the common-case network load. In this case, a bufferless network can attain nearly the same application performance while consuming less power, which yields higher energy efficiency.

For low-to-medium network load, a bufferless network has performance close to a conventional buffered network, because the deflection rate is low: thus, most flits take productive network hops on every cycle, just as in the buffered network. In addition, the bufferless router has significantly reduced power (hence improved energy efficiency), because the buffers in a conventional router consume significant power. However, as network load increases, the deflection rate in a bufferless deflection network also rises, because flits contend with each other more frequently. With a higher deflection rate, the dynamic power of a bufferless deflection network rises more quickly with load than dynamic power in an equivalent buffered

network, because each deflection incurs some extra work. Hence, bufferless deflection networks lose their energy efficiency advantage at high load. Just as important, the high deflection rate causes each flit to take a longer path to its destination, and this increased latency reduces the network throughput and system performance.

Overall, neither design obtains both good performance nor good energy efficiency at all loads. If the system usually experiences low-to-medium network load, then the bufferless design provides adequate performance with low power (hence high energy efficiency). But, if we use a conventional buffered design to obtain high performance, then energy efficiency is poor in the low-load case, and even buffer bypassing does not remove this overhead because buffers consume static power regardless of use. Finally, simply switching between these two extremes at a per-router granularity, as previously proposed [8], does not address the fundamental inefficiencies in the bufferless routing mode, but rather, uses input buffers for all incoming flits at a router when load is too high for the bufferless mode (hence retains the energy-inefficiency of buffered operation at high load). We now introduce our minimally-buffered deflection router which combines bufferless and buffered routing in a new way to reduce this overhead.

IV. MINBD: MINIMALLY-BUFFERED DEFLECTION ROUTER

The MinBD (minimally-buffered deflection) router is a new router design that combines bufferless deflection routing with a small buffer, which we call the "side buffer." We start by outlining the key principles we follow to reduce deflection caused inefficiency by using buffering:

1) When a flit would be deflected by a router, it is often better to buffer the flit and arbitrate again in a later cycle. Some buffering can avoid many deflections.

2) However, buffering every flit leads to unnecessary power overhead and buffer requirements, because many flits will be routed productively on the first try. The router should buffer a flit only if necessary.

3) Finally, when a flit arrives at its destination, it should be removed from the network (ejected) quickly, so that it does not continue to contend with other flits.

A. Basic High-Level Operation:

The MinBD router does not use input buffers, unlike conventional buffered routers. Instead, a flit that arrives at the router proceeds directly to the routing and arbitration logic. This logic performs deflection routing, so that when two flits contend for an output port, one of the flits is sent to another output instead. However, unlike a bufferless deflection router, the MinBD router can also buffer up to one flit per cycle in a single FIFO-queue side buffer.

The router examines all flits at the output of the deflection routing logic, and if any are deflected, one of the deflected flits is removed from the router pipeline and buffered (as long as the buffer is not full). From the side buffer, flits are re injected into the network by the router, in the same way that new traffic is injected. Thus, some flits that would have been deflected in a bufferless deflection router are removed from the network temporarily into this side buffer, and given a second chance to arbitrate for a productive router output when re-injected. This reduces the network's deflection rate (hence improves performance and energy efficiency) while buffering only a fraction of traffic.

B. Using a Small Buffer to Reduce Deflections

The key problem addressed by MinBD is deflection inefficiency at high load: in other words, when the network is highly utilized, contention between flits occurs often, and many flits will be deflected. We observe that adding a small buffer to a deflection router can reduce deflection rate, because the router can choose to buffer rather than deflect a flit when its output port is taken by another flit. Then, at a later time when output ports may be available, the buffered flit can re-try arbitration. Thus, to reduce deflection rate, MinBD adds a "side buffer" that buffers only some flits that otherwise would be deflected.

The side-buffer interfaces to the router pipeline in both the inject/eject and permute stages. First, it removes some deflected flits from the pipeline

after the permutation network assigns output ports, because the router only knows at this point which flits are deflected. Second, it eventually re-injects the flits that it buffers in the eject/inject stage, using a second instance of the injector that is placed before the ordinary injector (to give priority network access to buffered flits over new traffic). Finally, a "redirection" block is placed in the pipeline preceding the re-injection block in order to provide livelock-free delivery for buffered flits.

C. Injection and Ejection

A flit must enter and leave the network at some point. To allow traffic to enter (inject) and leave (eject), the MinBD router contains inject and eject blocks in its first pipeline stage. When a set of flits arrive on router inputs, these flits first pass through the ejection logic. This logic examines the destination of each flit, and if a flit is addressed to the local router, it is removed from the router pipeline and sent to the local network node.3 If more than one locally-addressed flit is present, the ejector picks one, according to the same priority scheme used by routing arbitration. Flits from the side buffer are re-injected before new traffic is injected into the network. However, note that there is no guarantee that a free slot will be available for an injection in any given cycle.

D. Prediction based flow control in MinBD

We would further improve upon the MinBD design, using the prediction flow control technique for the side buffer. The side buffer would generate status signals, which are sent out to neighbouring router switches.

We assume that there is an external control mechanism, which accumulates such status signals from neighbouring router switches, which helps in its decision making process of routing appropriate flit/s to the appropriate router switch. This mechanism would help control the congestion in the network, by predicting the routing flow.

V. IP CORE FPGA DESIGN IMPLEMENTATION METHODOLOGY

a. Goal: To develop a synthesizable IP core in HDL, for the input block (receiving packets) of the routing logic.

b. HDL:
  i. Design Description using Verilog-HDL

c. Verification Scheme:
  i. Functional Simulation using Xilinx ISE Simulator
  ii.Test bench for top level design using Verilog-HDL
  iii. Stimulus for testing IP Core
  iv. Simulation results / Timing diagram Analysis

d. FPGA Implementation:
  i. Design to be synthesized using Xilinx ISE Software.
  ii.Generate a design bit stream for FPGA device.
  iii. Demo the download of design bit stream on FPGA device.
  iv. No further verification on hardware / FPGA Kit
  v. FPGA kit will NOT be provided
  vi. Target Technology: Xilinx Spartan / Virtex Device

VI. CONCLUSION

MinBD combines deflection routing with a small buffer, such that some network traffic that would have been deflected is placed in the buffer instead. By using the buffer for only a fraction of network traffic, MinBD makes more efficient use of a given buffer size than a conventional input-buffered router. Its average network power is also greatly reduced: relative to an input-buffered router, buffer power is much lower, because buffers are smaller. Relative to a bufferless deflection router, dynamic power is lower, because deflection rate is reduced with the small buffer. And using prediction scheme injection rate of the packet also controlled, to improve performance.

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ANALYSIS OF SINGLE-PHASE Z-SOURCE INVERTER

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Abstract: This paper deals with the analysis of a single-phase Z-source inverter with common ground between the source and load. It gives the output same as that for full-bridge inverter for the specified input using only two switches. One-cycle control strategy is used as controlling technique for this topology. The topology is analysed using load and no load condition and verified by the simulation results.

Index Terms—Converter, one cycle control, single phase Z source inverter, Z source inverter.

1. INTRODUCTION

The traditional power converters are basically of two types: voltage-source converters and current source converters. These can be used in single phase as well as three-phase power converters. This paper mainly focuses on a single-phase power conversion. The traditional voltage-source converters and current-source converters have certain disadvantages associated with them. In case of voltage-source (V-source) converters, it acts as a buck (step-down) converter for DC to AC power conversion and as a boost (step-up) converter for AC to DC power conversion. In case of current source (I-source) power converter, it acts as a boost converter for DC to AC power conversion and as a buck converter for AC to DC power conversion. Thus, V-source and I-source power converter can be used as either as a boost or a buck converter and not as a buck-boost converter. Moreover, in case of a three-phase power conversion, if both the upper and lower switches of the same leg are

simultaneously turned ON either by purpose or by electromagnetic interference, a shoot-through occurs and the converter is damaged [1].

For single-phase power conversion, the basic topologies used include the bridge topologies. Fig. 1(a) and (b) shows full bridge inverter and half bridge inverter topologies resp. In case of full bridge inverter, four switches are used to get desired output voltage, whereas in case of half bridge inverter topology only two switches are used. But the output voltage obtained in half bridge inverter topology is half the input voltage.
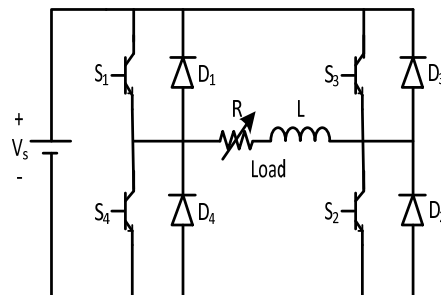
Fig. 1 (a): Full bridge inverter
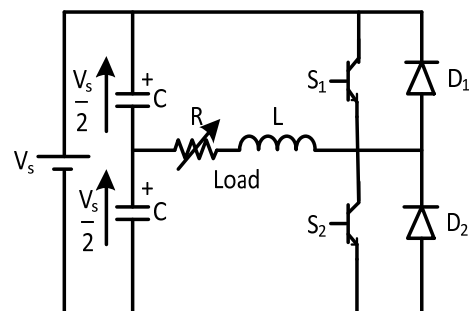
Fig. 1 (b): Half bridge inverter

Due to the use of more switches, full bridge inverter topology is costly. All the disadvantages mentioned above of the traditional V-source, I-source and bridge converter topologies are

overcome by the use of Z-source (impedance source) converters.

2. Z-SOURCE CONVERTER

The impedance source or Z-source converter provides the unique features which overcomes the disadvantages of the traditional voltage source converters and current source converters. Fig (2) shows the basic structure of Z-source converter topology. It employs the unique impedance network which is used to couple the converter circuit to the power source (may be voltage source or current source), load or another converter. It can be used for implementing DC to AC, AC to DC, DC to DC or AC to AC power conversion with both the step-down and step-up features [1].

In basic topologies, Z-source networks are symmetrical. The basic impedance network consists of two identical inductors L_1 and L_2 and two identical capacitors C_1 and C_2 connected in X-shape as shown in Fig.2 providing coupling between the power source and load. The impedance network is the energy storing element for the converter. The same impedance network can be used in a single-phase or three-phase Z-source converter topology. Depending on the type of power supply used, Z-source converter is either voltage-fed Z-source converter or current-fed Z-source converter. In case of 3-phase converters, a voltage-fed Z-source converter has an unique feature of allowing both the upper and lower power switches of the same phase-leg to be turned ON simultaneously without damaging the converter [2].
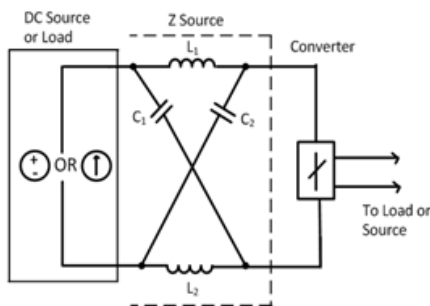
Fig. 2: Basic structure of Z-source converter

(a)

(b)
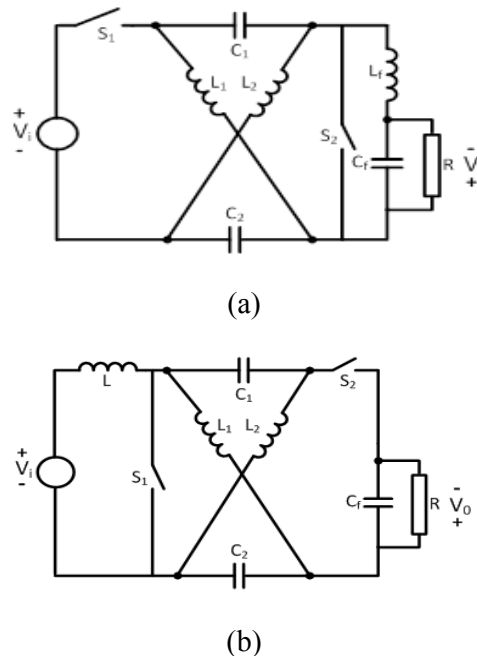
Fig. 3: 1-ph Z-source converter topologies
(a) Voltage-fed (b) Current-fed

The single-phase Z-source inverter consists of two switches and impedance source network giving the output same as that of the full bridge inverter with reduced number of switches. Fig. 3(a) and 3(b) shows the basic topologies of single-phase Z-source converter: (a) Voltage-fed and (b) Current-fed resp. The two switches S1 and S2 are tuned ON and OFF in complement. The relationship between the voltage gain and duty ratio D of the voltage-source and current-source topologies, respectively, is given by

$$\frac{Vo}{Vi} = \frac{D}{2D-1} \qquad (1)$$

and $$\frac{Vo}{Vi} = \frac{2D-1}{D-1} \qquad (2)$$

From equation (1), when voltage gain is plotted against duty ratio, it shows that the Z-source converter acts as both step-up and step-down converter. This is a unique feature of Z-source inverter as compared to other inverters. From fig 3(a) and 3(b), it can be seen that these topologies need separate grounding for source and load and hence it cannot be used in cases where a common grounding is required for source and load. This paper deals with a single-phase Z-source inverter topology with common ground between the source and load [3]. One-cycle controlled strategy is adopted as a control strategy for this topology [4].

3. SINGLE-PHASE Z-SOURCE INVERTER TOPOLOGY WITH COMMON GROUND

Fig.4 shows the single-phase Z-source inverter topology having common ground between the input and the output. The Z-source network employed in this topology is unsymmetrical unlike the basic Z-source inverter topology discussed above. The proposed topology constitutes an unsymmetrical impedance network consisting of two inductors L_1 and L_2 and a single capacitor C, DC voltage source V_i, two switches S_1 and S_2 and filter capacitor C_f. This topology uses only two switches unlike full-bridge inverter which uses 4 switches while keeping the voltage transfer ratio the same as for the full-bridge inverter topology.

The two switches S_1 and S_2 act in complement to each other. Assuming 'D' to be the duty ratio and 'T' to be the switching period, switch S_1 is ON for DT period and switch S_2 is ON for the period (1-D)T. So, there exist two switching states in one switching cycle which are shown in Fig. 5(a) and 5(b).
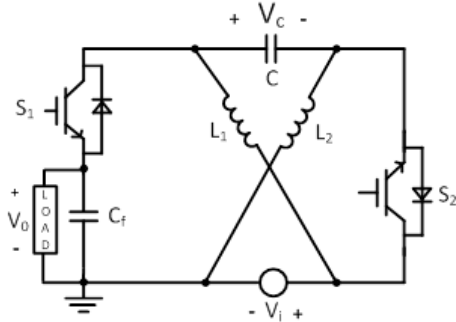
Fig.4: 1-ph Z-source inverter topology with common ground
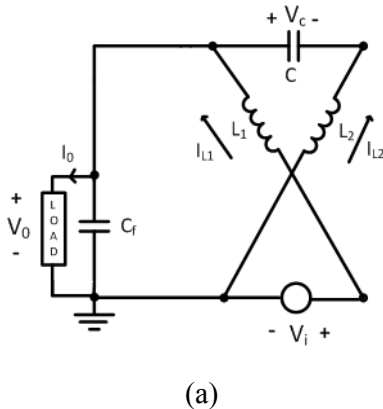
(a)
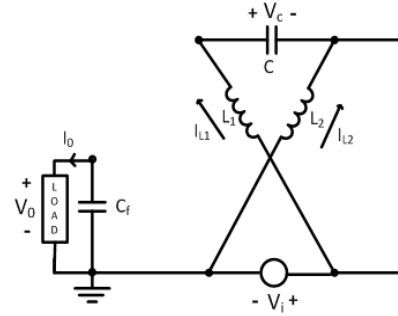
(b)

Fig. 5: Equivalent circuits (a) State 1 (b) State 2

For the period DT, from fig. 5(a), the equations can be written as,

$$L_1 \frac{di_{L1}}{dt} = V_i - v_o$$

$$L_2 \frac{di_{L2}}{dt} = v_c - v_o$$

$$C \frac{dv_c}{dt} = -i_{L2}$$

$$C_f \frac{dv_o}{dt} = i_{L1} + i_{L2} - i_0 \qquad (3)$$

For the period (1-D)T, from fig. 5(b), the equations can be written as,

$$L_1 \frac{di_{L1}}{dt} = -v_c$$

$$L_2 \frac{di_{L2}}{dt} = -v_i$$

$$C \frac{dv_c}{dt} = i_{L1}$$

$$C_f \frac{dv_o}{dt} = -i_0 \qquad (4)$$

Averaging equations (3) and (4) over time period T, we write,

$$L_1 \frac{di_{L1}}{dt} = D(V_i - v_o) - (1 - D) v_c$$

$$L_2 \frac{di_{L2}}{dt} = D(v_c - v_o) - (1 - D) v_i$$

$$C \frac{dv_c}{dt} = -D i_{L2} + (1 - D) i_{L1}$$

$$C_f \frac{dv_o}{dt} = D(i_{L1} + i_{L2}) - i_o \qquad (5)$$

From the above equations and the circuit, the steady state equations can be written as,

$$v_C = V_i \qquad (6)$$

$$\frac{v_o}{V_i} = \frac{2D-1}{D} \qquad (7)$$

$$i_{L1} = i_o \qquad (8)$$

$$i_{L2} = \frac{1-D}{D} i_{L1} \qquad (9)$$

From equation (7), it can be seen that the network performs buck-boost conversion with changing polarity when D < 0.5. Also, it acts as a buck inverter for D > 0.5 with the output polarity same as that of the input. For small value of duty ratio, the circuit is affected more by external factors. For this topology, duty ratio ranges from 1/3 to 1 and hence it acts as a buck inverter. From equation (9), we get the relation between two inductor currents, which depends on the duty ratio. For the minimum value of duty ratio, we get maximum unbalance in the two inductor currents as $i_{L2} = 2\ i_{L1}$.

From fig.4 and equation (6), we can write the equation for voltage across switch S1 as,

$$v_{S1} = v_C + V_i - v_o = 2\ V_i - v_o \qquad (10)$$
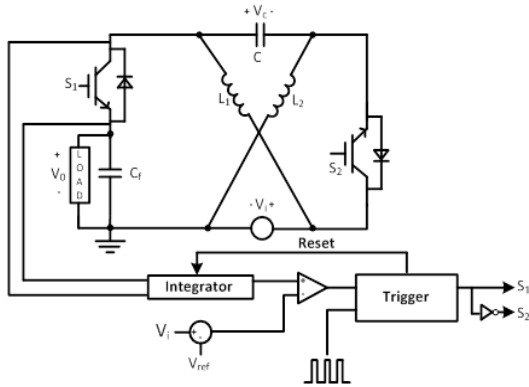
Fig.6: Z-Source inverter with one-cycle control strategy.

Thus, the voltage across the switches is more.

The elements of the impedance networks are designed based on the ripple contents. Fig. 5(b) shows that the capacitor C is charged by the current i_{L1} in the time interval (1-D)T. Thus, the voltage ripple across the capacitor is given by

$$\Delta V_C = \frac{i_{L1}(1-D)T}{C} \cong C = \frac{i_{L1}(1-D)T}{k_v * v_i} \qquad (11)$$

Also, the inductor current ripple can be given as,

$$\Delta i_L = \frac{Vi*D*T}{L} \cong L = \frac{Vi*D*T}{k_i * i_L} \qquad (12)$$

Where, k_v and k_i are capacitor voltage and inductor current ripple factors respectively.

4. ONE-CYCLE CONTROL THEORY

Using one-cycle control strategy, the power source perturbations can be minimised and highly efficient constant frequency control can be achieved. It corrects switching error on one switching cycle. Duty ratio of the switch depends on the states of the current switching cycle. Fig.6 shows Z-Source inverter with one-cycle control strategy.

The voltage across switch S1 is sensed and fed to the integrator. S1 is switched OFF and S2 is switched ON by the clock signal. Thus, the integrator voltage is given by,

$$v_{int} = k \int_0^t (V_{S1} dt)$$

$$= k \int_0^{(1-D)T} (v_C + V_i - v_o) dt \qquad (13)$$

The integrator will reset when the integrator value reaches $V_i - V_{ref}$ and S1 will be switched ON.

$$v_{int} = V_i - V_{ref} \qquad (14)$$

The average value across the switch S1 is given by

$$\overline{V_{S1}} = \frac{1}{T} \int_0^{(1-D)T} \left(v_C + V_i - v_o \right) dt = K(V_i - V_{ref}) \qquad (15)$$

Where, $K = \frac{1}{kT} = 1$

The average voltage across inductor L, in steady state, is zero.

$$\overline{V_{S1}} = V_i - v_o$$
(16)

Comparing equations (15) and (16)

$$V_i - V_{ref} = V_i - v_o$$

Thus, $\qquad V_{ref} = v_o \qquad$ (17)

5. SIMULATION RESULTS

Simulations have been performed to analyse the proposed topology. The z-network parameters used are: Inductors L_1 and $L_2 = 2$ mH, capacitor C = 220 μF. Other parameters are: Input DC voltage $V_i = 350$ V, output voltage v_o = 230 V, output voltage frequency is 50 Hz, switching frequency is 25 kHz and filter capacitance $C_f = 25$ μF. The load resistance is 60 Ω. Fig.8 shows the simulation results for load resistance R = 60 Ω. Also, to analyse the effect of mutual inductance, coupling of factor of 0.5 is used for the same parameters. Fig.9 shows the simulation results for load resistance R = 60 Ω with mutual inductance. From fig.8 and fig.9, it can be seen that the ripples are reduced to the great extent by the use of mutually coupled inductors. Fig.10 shows the simulation results for no load with mutual inductance.
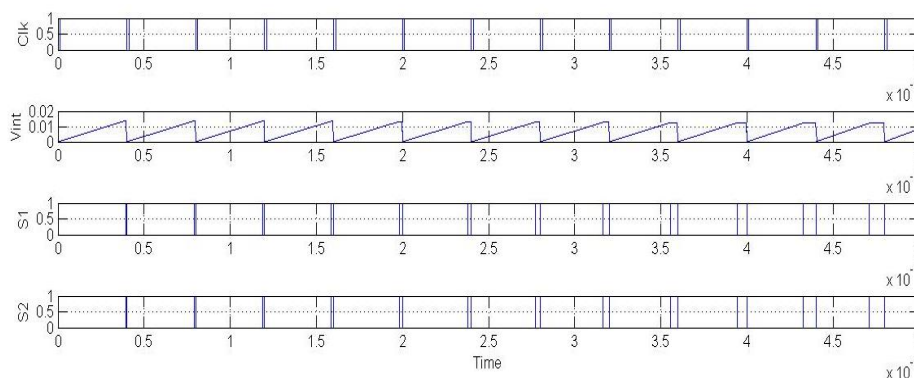
Fig.7: Principle Waveform for one-cycle control
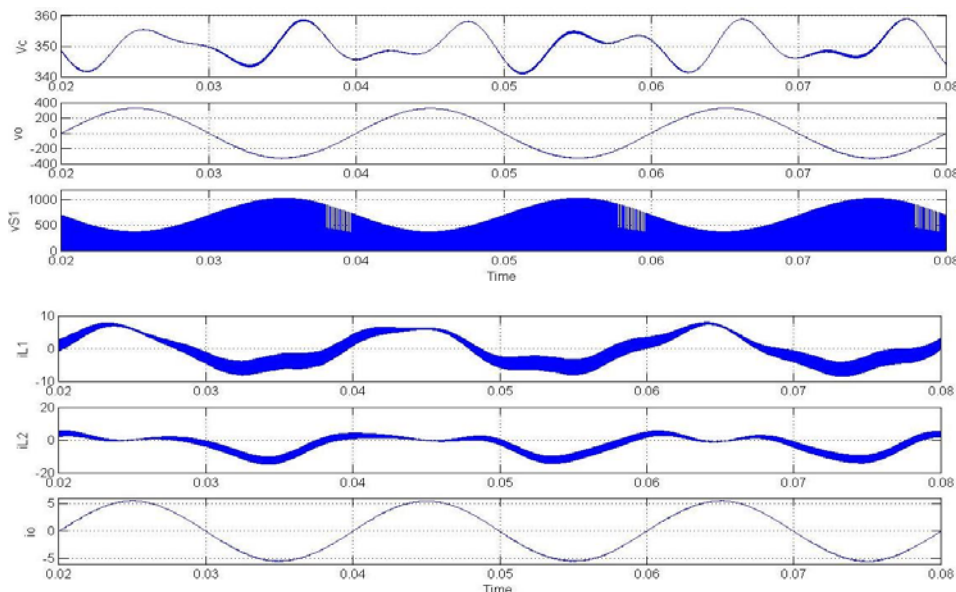
Fig 8: Simulation result for load resistance R = 60 Ω without mutual inductance.
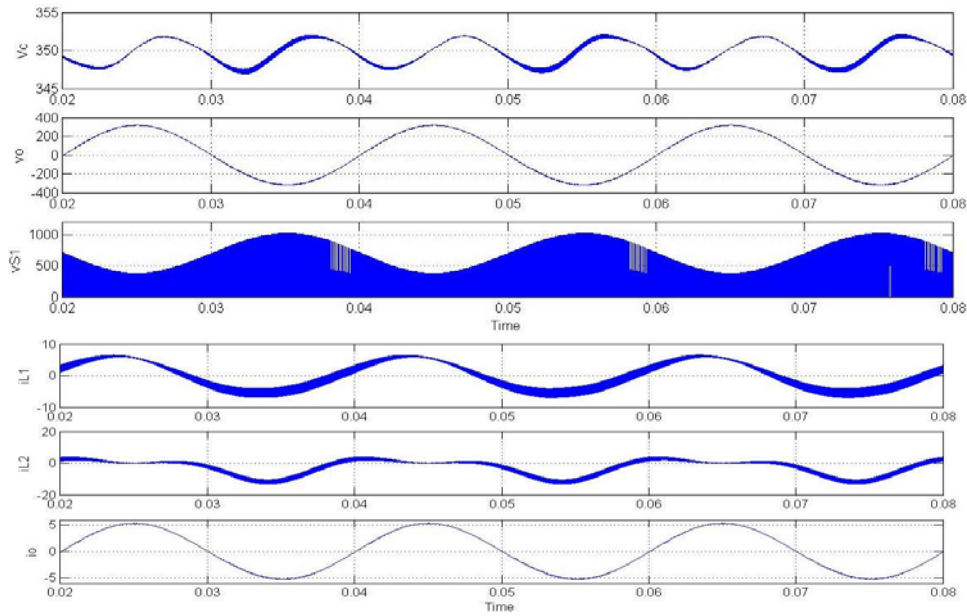
Fig 9: Simulation result for load resistance R = 60 Ω with mutual inductance.
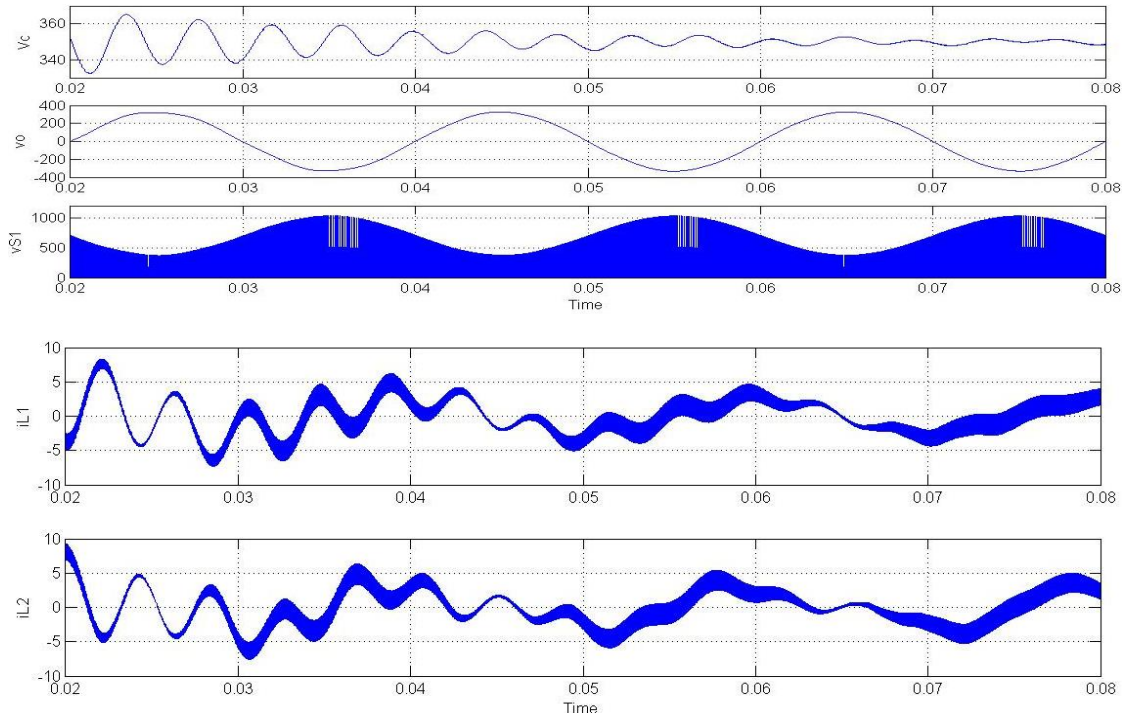
Fig. 10: Simulation results for no load with mutual inductance.

6. CONCLUSION

A single-phase Z-source inverter topology with common ground between the supply and load has been analysed. The topology is analysed by network analysis and simulation also performed to check the result. The effect of mutual inductance in Z-source network has also been analysed.

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COUNTING OF WAGONS IN NIGHT VIDEO BASED ON BACKGROUND SUBTRACTION

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Abstract— A novel approach for train wagon counting during night time is proposed in this paper. Different from traditional background subtraction and segmentation algorithms, this method subtracts only central reference line pixel values from the pixel values of the reference background at the same location. This increases the processing speed of the algorithm as well as efficiency of the system. The RGB pixel values are considered for background subtraction. The pixel difference values determine the segmentation of background and the foreground objects, which here in this case are railway wagons.

Index Terms—Segmentation, Background Subtraction, Object counting.

I. INTRODUCTION

In most of the computer vision related applications, detection and identification of moving object from a given video is critical task. Most common approaches include background subtraction method which is used in number of applications like surveillance systems, remote sensing, in biomedical fields, etc for monitoring and tracking purpose. It is mostly based on the prior background model and comparison of video frames with background model is carried out. Any deviation from background model is considered as the foreground object. Advantage of such types of method is that it is not dependent on the prior knowledge about shape and size of objects. Most of the background subtraction methods are sensitive to illumination changes. In many cases background is not stationary. It may change with time during a day or due to objects in background like trees, mountains or buildings. Lots of work is done in this area. Early approaches are based on Gaussians mixture model which depends on the distribution of pixels. Model stability and convergence problems were seen in such methods. Dar-Shyang Lee [1] proposed effective Gaussian Mixture Learning method which improves convergence rate and stability up to some extent. Memory consumption and processing time, these are some concerns related with the mixtures of Gaussian methods which may leads to errors. Probability based Robust Object Segmentation System for Background Extraction is developed by Chung-Cheng Chiu, Min-Yu Ku, and Li-Wey Liang [2]. Their algorithm detects objects under different illumination changes with reduction in memory consumption and minimizing processing time with further scope for including object tracking and recognition. Yumiba, Miyoshi, Fujiyoshi [3] developed an algorithm which is based on Spatio-Temporal Texture. Their method covers a dynamic background change and is based on *"Space-Time Patch features"*. Their method is robust against global and local background change and it is based on only detecting presence or absence of object but it doesn't reveal any information related to objects like position or size. To detect objects under sudden illumination changes, Cheng, Huang, and Ruan [4] proposed a system in which they have used three modules- background

model module, illumination evaluation module and object detection module. Their algorithm is compared with approaches like MTD, SSD and MSDE. Their method calculates adaptive threshold for object segmentation with future scope for improving adaptive threshold for better detection. Another approach uses foreground adaptive background subtraction method where McHugh, Konrad, Saligrama [5] have used nonparametric background model along with foreground model based on small spatial neighborhood to improve sensitivity. They have also used Markov model to change labels to improve spatial coherence of the detections. This is mainly done in order to improve threshold of detection. However, proper initial labeling is needed for proper estimation. Recent approach includes work done by Shih-Chia Huang [6] for automatic surveillance system. Their extensive works based on detection of moving objects by using background modeling (BM) module, an alarm trigger (AT) module, and an object extraction (OE) module. For our proposed BM module, a unique two-phase background matching procedure is performed, AT module saves the effort by eliminating unnecessary examination of the entire background region, the OE module forms the binary object detection mask for detection of moving objects.

In our proposed method, object of interest is wagons i.e we are interested in counting no of moving wagons from a given video frames. Our aim is to track and count no moving wagons under different illumination condition especially during night time using background subtraction method. Most of the present algorithms useful for detecting moving object during day time. They are very much robust for detecting object when there is sufficient illumination but their performance is not very much accurate when there is insufficient light. During night time, background and object of interest both appears dark which leads to segmentation problem. Our work basically concentrated on this problem. Challenge is to develop such system to determine threshold which gives better results under circumstances mentioned above.

Paper is organized as follows: Following sections gives details about proposed algorithm along with results. Conclusion and future scope is given at last section followed by the references.

II. PROPOSED METHOD

A. Algorithm

The paper describes here an automated train monitoring system. To count the number of wagons in a freight train, an automated vision system is developed here. The train video of moving freight train from side view is captured as input to the system, which is further processed by using image processing techniques. The videos captured are during night and contain different imaging conditions i.e. cloudy, rainy etc. Also the background of the video can be plain or can contain clutter as well as it can be varying with time. The main challenges to the development of the system include illumination changes, varying background conditions and real time constraints on processing.

The method proposed in this paper considers only night time videos. The videos used for experiments consist of train wagons moving in backward or forward direction. The train speed changes abruptly. The train sometimes halts for any random time period. The background in the videos contain non-stationary objects such as tree leaves. Swaying of the tree leaves due to breeze also affects the RGB values of the background, thus indicating change in the foreground. Some of the videos contain noise due to improper illumination source and low resolution. The proposed algorithm is robust and addresses all the above mentioned environmental conditions and abrupt change in the train movements. The proposed algorithm is divided into five steps; first is video acquisition, second is background reference frame extraction. The third step is Central reference line detection. Next steps are RGB value extraction then background subtraction and the last step consists of wagon counting. The proposed method is explained in the following sub-section:

Video Acquisition:

First step is video acquisition. The videos containing the side view of railway wagons during night time is acquired first. The proposed method can be implemented for real time video

processing. For experimental purpose, the pre-recorded video files are used in this paper. The acquired video sequence is first loaded into the database. The video file consists of consecutive image frames. As the system starts video acquisition, the width and height of the image frame are stored for scanning the frame. The image frames from the video sequence are then extracted and saved on the system. For each consecutive image frame, and for the total no. of rows and columns, the entire image frame is scanned and the pixel intensity values are stored in the database for further processing.

Background Reference Frame extraction:

In conventional background subtraction methods, the first image frame of the video is saved as the background. Alternatively, to make the system robust to dynamic or time varying background, first few image frames from the video are saved and then the average of all the pixels of the image can be taken and is considered as the reference background image. In the proposed method, the night time videos used as the database have poor illumination conditions. Thus, the background of the video does not change as compared to the foreground. As mentioned in the previous sub-section, the night time video contains the dynamic background like swaying tree leaves. To address the problem of such time-varying background, first 50 image frames of the video are acquired first and then for the total no. of rows and columns, these pixel intensity values at each pixel is stored. For every pixel location in the image frame, the summation of the intensity values is taken and then average of this addition is saved in the respective pixel location. Thus, a new image is obtained containing the average intensity pixel values of the first 50 frames. The new background reference image is obtained by the following averaging operation:

$$f'(i,j) = \sum_{i=0}^{M-1} \sum_{j=0}^{N-1} \left[\left(\sum_{k=0}^{P-1} f(i,j) \right) \Big/ P \right]$$

(1)

This new image is taken as background reference image frame for further processing. The size of the reference frame is saved for scanning the image frames.

Central reference line detection:

In previously proposed background subtraction methods, the consecutive image frames are subtracted from the previous image frames or from the reference image frame. This increases the processing time, as to subtract entire consecutive image frame from the reference frame, we need to scan the entire image for total height and width of the image frame and then perform the image subtraction pixel-by-pixel. In our proposed method, instead of considering the entire image frame, only the pixels belonging to central reference line of the image are scanned for any foreground change. The main purpose of the algorithm is to find the gap between the consecutive wagons and then count the no. of wagons. The central reference line of the image frame scans the areas of railway wagons passing in the video. The value of the width of the background reference image frame is used for scanning the image horizontally and the value of the height of the reference image frame is used to get the height of the central reference line, as the central reference line is obtained by dividing the height by two. This central reference line is then used in the next step for RGB value extraction process.

RGB Value Extraction Process:

In the next step, the RGB values of the background reference image for the central reference line are stored in the class and then decomposed into three different R, G and B values for background subtraction. As the consecutive video frames appear and the railway wagons start to appear, there is change in the RGB value of the foreground. For each consecutive frame, the RGB value only for the central reference line is stored into a class. For each new frame, the RGB values are then decomposed into separate R, G and B values from the class. Here ends the RGB value extraction process.

Background Subtraction:

In previously proposed methods, first the binarization of the image frames is performed and then the new image frame pixel intensities are subtracted from those of the background frame. We have considered the RGB values of the video frames for background subtraction. In binarization, thresholding technique is used to assign the binary value to the pixel intensity. If

the RGB value of the image frame is above certain threshold then it is assigned as 0 or 1. In this process of binarization, due to thresholding, the pixel intensity information may get lost. The pixel intensity values play vital role because of poor illumination conditions. To avoid it, in our paper we have considered only RGB values. The R, G and B values of the reference background frame are then subtracted from the respective R, G and B values of the consecutive video frames and then calculated differences are saved as R, G and B difference values. Even though the background remains considerably static, there may exist some noise or clutter in the background or there can be some illumination change due to light source. To tackle such scenarios, the threshold is set for the R, G and B difference values. If the difference values fall within that range, then the change in the foreground is considered as negligible and can be ignored.

This operation is performed as follows:

$$f'(i,j)(t+1)$$
$$= \begin{cases} f(i,j)(t) & if \ |diff| < th \\ f(i,j)(t+1) & otherwise \end{cases}$$
$$(2)$$

Where 'th' stands for threshold value and the value of diff is calculated as:

$$diff = f(i,j)(t+1) - f(i,j)(t)$$
$$(3)$$

Wagon counting algorithm:

This sub-section explains the wagon counting algorithm used in the proposed method. Two separate difference values are stored from the background subtraction; one for the gap between the wagons and the other for the length of the wagon. The purpose behind two separate difference values is to evaluate the length of the gap between the wagons and to check the length of the wagon itself. Then on the basis of these lengths, the wagons are counted. If the difference in the background and foreground frame falls within the threshold, then the counter for the difference value for the gap is increased. And if the difference value is greater than the threshold, it indicates that there is change in the foreground and the train wagon has arrived. Such change in the foreground pixel is indicated by the yellow color on the central reference line. Also, the counter for the difference value for the length of

the wagon is increased. Every time the counter for gap and wagon length is increased, the counters are checked for another threshold values. Once the counter for gap is reached, the next wagon is counted and added to the no. of bogies counted previously. Also, the gap counter is set to zero again. Similarly, once the counter for entire wagon length is reached, it is again set to zero to check for next gap between the bogies. For the night time videos, the main challenge is to deal with the background illumination. During night time, to illuminate the objects, the only source is the light source used along with the camera. Unlike for day time videos, the natural day light illuminates the foreground objects as well as the background. While processing the day time videos, the background may vary with time. Thus after extraction of first few frames, if the background varies, then this variation in background may be considered as change in the foreground, finally affecting the results. Thus, the algorithm considering only first few frames for the background subtraction fails in such cases. The same problem is encountered in the night time videos, where the light source illuminates the background as well as foreground properly. In such cases, if the RGB values of the foreground objects resemble with those of the background and fall within the pre-decided threshold, then there are chances of the foreground objects getting counted as the background. To address this problem, the reference background can be updated after pre-decided no. of frames.

III. EXPERIMENTS AND RESULTS

The video database of night time contains the side view of the railway wagons going in forward or backward direction with varying frame sizes. The resolutions of the frames are 1280 x 960, 1280 x 800. The frame rates are 5.03 FPS, 10 FPS. The pre-recorded videos are in .mp4 and .avi formats. The distance of the camera from train is varying in all videos. It is approximately 15-20 feet. The height of the camera is 10-15 feet from ground. The videos are captured with different background and environmental conditions with the light source for illumination purpose. Following table shows the details of the video database:

Video Name	Resolution
CTPS_Night_Forward_Stream	1280*960
CTPS_Night_Reverse_Stream2	1280*960
Panvel_NightStream1	1280 x 800
Panvel_NightStream2	1280 x 800

The quality of the results is checked by structural similarity (SSIM), peak signal to noise ratio (PSNR) and root mean square error (RMSE) values.

The quality of the image frames are checked by SSIM index. The SSIM checks for the structural similarity of the distortion free images with the noisy images. It is further extension of the traditional quality index measurement techniques i.e. PSNR and RMSE. The PSNR value calculates peak signal to noise ratio of the image in dBs. The high value of PSNR indicates the good quality of image frame, ideal value is infinity. As seen from the results, we get PSNR value in the range of 60dB. The RMSE assesses the quality of the resultant images. The smaller RMSE value better is the quality and we get very small range of RMSE values.

The SSIM is calculated on the basis of formula:

$$SSIM(i,j) = \frac{(2\mu_i\mu_j + c_1)(2\sigma_{ij} + c_2)}{(\mu_i^2 + \mu_j^2 + c_1)(\mu_i^2 + \mu_j^2 + c_2)}$$

(4)

Where μ represents the average value and σ represents the variance value and c is the factor for stabilization.

The RMSE is calculated as follows:

$$MSE = \frac{\sum(IMG_{orig} - IMG_{noisy})^2}{m}$$
$$RMSE = \sqrt{MSE}$$

(5)

where the MSE is calculated by subtracting noisy image from original image and then normalizing it by factor 'm'. The RMSE value is calculated by taking square root of MSE.

The PSNR is calculated by following formula:

$$PSNR = 20 \log_{10}\left(\frac{MAX}{RMSE}\right)$$

(6)

where Max represents the maximum illumination pixel intensity.

After applying the proposed algorithm, we are able to segment the railway wagons from the background and count them successfully and correctly. The quality index values of RMSE, SSIM and PSNR for the used night time video are tabulated below:

Video Name	RMSE	SSIM	PSNR
CTPS_Night_Forward_Stream1	0.0118	0.9999	86.66db

The results are as shown in the figure below:

α =5, RMSE =0.012911 DTV90-PSNR85.9119MSSIM0.99998

Swaying tree leaves detected as foreground

Counted train wagons and foreground detection
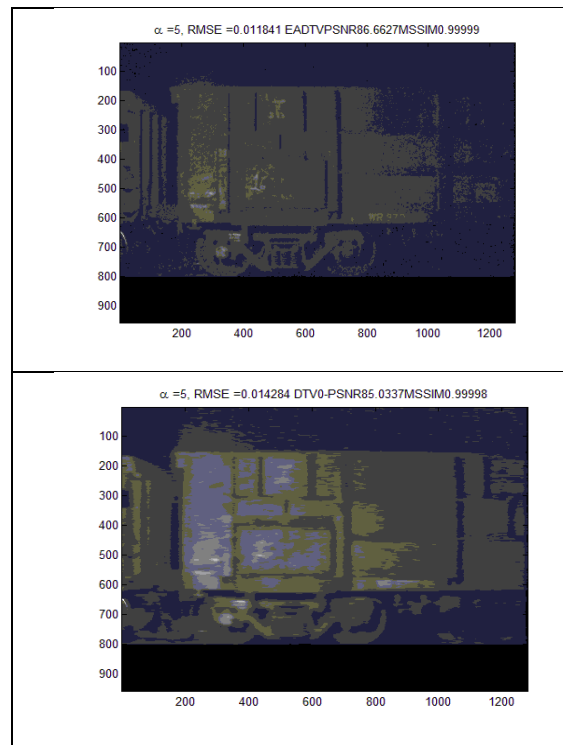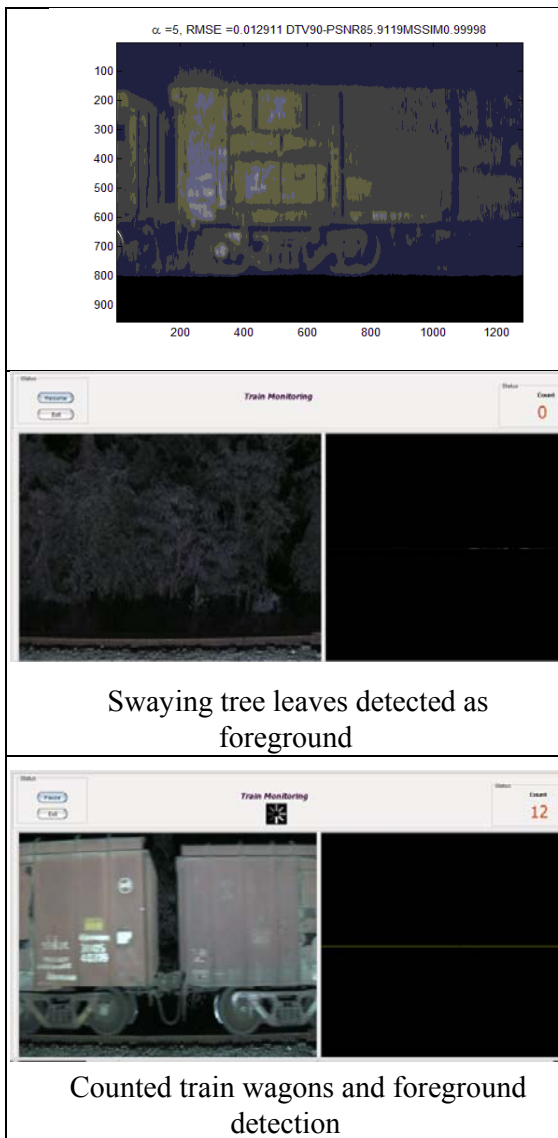
IV. CONCLUSION AND FUTURE WORK

We have proposed and implemented video based automated system for train monitoring for counting the number of wagons of the train. This work presents a novel approach in detecting and counting the railroad cars in continuous train video images, which were recorded using a camera.

The proposed algorithm gives good results for the noisy night videos of railway wagons. The values of quality index parameters indicate same. The processing time for the algorithm is very fast as compared to traditional background subtraction algorithms. The same algorithm can be applied to the day time videos by adding the adaptive threshold algorithm. According to the illumination present in the video frames, the adaptive threshold is changed and the same algorithm can be implemented for both day and night time videos. This can be implemented as the extension of the method proposed in this paper.

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TOPOLOGY-AWARE QUALITY-OF-SERVICE SUPPORT IN HIGHLY INTEGRATED CHIP MULTIPROCESSORS

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Abstract— With increase in integration density and complexity of the system-on-Chip (SOC), the conventional interconnects are not suitable to fulfill the demands. As CMP-level quality of service(QOS) support becomes necessary to provide performance isolation, service grantees & security. The application of traditional network technologies in the form of Network-on-Chip is a potential solution. NoC design space has many variables. Selection of a better topology results in lesser complexities and better power-efficiency. In the proposed work, key research area in Network-on-chip design targeting communication infrastructure specially focusing on optimized topology design is worked upon. The simulation is modeled using a conventional network simulator Network simulator-2 (NS-2), in which by selecting proposed Topology gives reduction in traversing the longest path is observed. We evaluate several topologies for the QOS-enabled shared regions, focusing on the interaction between network-on-chip (NOC) and QOS metrics. We explore a new topology called Destination Partitioned Subnets (DPS), which uses a light-weight dedicated network for each destination node. On synthetic workloads, DPS nearly matches or outperforms other topologies with comparable bisection bandwidth in terms of performance, area overhead, energy- efficiency, fairness, and preemption resilience.

Index Terms— NoC, SoC, Routing,NS-2 simulator.

I. INTRODUCTION

The abrupt emergence of multi-core chips and their rapid proliferation have left researchers and industry scrambling for ways to exploit them. Two notable paradigms have arisen for monetizing CMPs – server consolidation and cloud computing. The former allows businesses to reduce server costs by virtualizing multiple servers on a single chip,thereby eliminating dedicated hardware boxes for each individualserver. The latter enables delivery of various clientservices from remote (i.e., "cloud") servers. Since a single CMP can serve multiple users concurrently, hardware, infrastructure and management costs are reduced relative to a model where each user requires a dedicated CPU Unfortunately, these novel usage models create new system challenges and vulnerabilities. For instance, in a consolidated server scenario, different priorities may be assigned to different servers.

Thus, web and database servers for external customers could have a higher priority than intranet servers. But as multiple virtualized servers may be executing concurrently on a multi-core chip, traditional OS level preemptive scheduling policies can fail at properly enforcing priorities of different VMs competing for shared resources. In a cloud setting, multiple users may be virtualized on to a common physical substrate, creating a number of new concerns, including inadvertent interference among the different users, deliberate denial-of-service attacks, and side channel information leakage vulnerabilities. Researchers have recently demonstrated a number of such attacks in areal-world setting on Amazon's EC2

cloud infrastructure, highlighting the threat posed by chip-level resource sharing on a public cloud. Today's CMPs lack a way to enforce priorities and ensure performance-level isolation among the simultaneously executing threads. Inter-thread interference may occur in any of the shared resources present on a CMP, including caches, memory controllers, and the on-chip network. Researchers have suggested using on-chip hardware quality-of-service (QOS) mechanisms to enforce priorities, limit the extent of interference, and provide guarantees for threads sharing a substrate.

In this work, we take a network-centric, topology-aware approach to chip-level quality-of-service. To reduce performance, area, and energy overheads of network-wide QOS support, we propose to isolate shared resources, such as memory controllers and accelerator units, into dedicated regions of the chip. Hardware QOS support in the network and at the end-points is provided *only* inside these regions.

The focal point of this paper is the organization of the shared region.

We evaluate Destination Partitioned Subnets (DPS), a new topology we propose in this work. DPS uses a dedicated sub network for each destination node, enabling complexity-effective routers with low delay and energy overhead. All topologies show good fairness and experience little slowdown in the face of adversarial workloads with high preemption rates. On synthetic workloads, DPS consistently matches or outperforms mesh-based topologies in terms of performance, energy efficiency,and preemption resilience.

As the network communication latency depends on the characteristics of the target application, computational elements and network characteristics (e.g. network bandwidth and buffer size [2]. First of all the target applications and their associated traffic patterns and bandwidth requirements for each node in the network is determined. This application partitioning and knowledge of overall system architecture significantly impact the network traffic and helps determine the optimal network topology. Optimal network topology creates immense impact of design cost, power and performance and helps designers to choose effective and efficient routing algorithms and flow control scheme to manage

incoming traffic. The design space of a NoC is very large, and includes topology choice (mesh, torus, star, etc.), circuit switched or packet switched, and other parameters (link widths, frequency, etc.). Because the traffic patterns of most SoCs can be known, a custom generated network topology and physical placement of components yields better performance and power than a regular-pattern network [4]. A NoC's buffers and links can consume near 75% of the total NoC power [5], thus there is significant benefit to optimizing buffer size, link length and bandwidth of a NoC design. Generally speaking, determining the optimal topology to implement any given application does not have a known theoretical solution. Although the synthesis of customized architectures is desirable for improved performance, power consumption and reduced area, altering the regular grid-like structure brings into the picture significant implementation issues, such as floor planning, uneven wire lengths (hence, poorly controlled electrical parameters), etc. Consequently, Exploring Alternative Topologies for Network-on-Chip Architectures ways to determine efficient topologies that trade-off high-level performance issues against detailed implementation constraints at micro- or nano-scale level need to be developed.

II. BACKGROUND

The early work and basic principles of NoC paradigm were outlined in various seminal articles, for example [7-17] and few text books [18-20]. However, the aforementioned sources do not present many implementation examples or conclusions. Networking concepts from the domains of telecommunication and parallel computer do not apply directly on chip. From a networking perspective, they require adaptation because of the unique nature of VLSI constraints and cost e.g. area and power minimization are essential; buffer space in on-chip switches are limited, latency is very important, etc. At the same time, there are new degrees of freedom available to the network designer, such as the ability to modify the placement of network endpoints. From the view point of VLSI designer, many well understood problems in the real aim of chip development methodology get a new slant when they are formulated for a NoC based system, a new trade-offs need to be comprehended. Therefore, the

field offer opportunities for noble solutions in network engineering as well as system architecture, circuit technology, and design automation. [6] Current complex on-chip systems are also modular, but most often the modules are interconnected by an on-chip bus. The bus is a communication solution inherited from the design of large board- or rack-systems in the 1990's. It has been adapted to the SoC specifics and currently several widely adopted on- chip bus specifications are available [31-34]. While the bus facilitates modularity by defining a standard interface, it has major disadvantages. Firstly, a bus does not structure the global wires and does not keep them short. Bus wires may span the entire chip area and to meet constraints like area and speed the bus layout has to be customized [35]. Long wires also make buses inefficient from an energy point of view [36]. Secondly, a bus offers poor scalability. Increasing the number of modules on-chip only increases the communication demands, but the bus bandwidth stays the same. Therefore, as the systems grow in size with the technology, the bus will become a system bottleneck because of its limited bandwidth. Recently, network-on-chip (NoC) architectures are emerging as a candidate for the highly scalable, reliable, and modular on-chip communication infrastructure platform [11]. The NoC architecture uses layered protocols and packet-switched networks which consist of on-chip routers, links, and network interfaces on a predefined topology. There have been many architectural and theoretical studies on NoCs such as design methodology [10], [11], topology exploration [21], Quality-of- Service (QoS) guarantee [22], resource management by software [23], and test and verifications [24]. In large-scale SoCs, the power consumption on the communication infrastructure should be minimized for reliable, feasible, and cost-efficient implementations. However, little research has reported on energy- and power-efficient NoCs at a circuit or implementation level, since most of previous works have taken a top-down approach and they did not touch the issues on a physical level, still staying in a high-level analysis. Although a few of them were implemented and verified on the silicon [25], [26],they were only focusing on performance and scalability issues rather than the power-efficiency, which is one of

the most crucial issues for the practical application to SoC design.

III METHODOLOGY

Network-on-Chip is a new paradigm for interconnecting today's heterogeneous IP cores based System-on-Chips (SoCs). In SoC's IP Cores are connected to network of routers using network interfaces and network is used for packet switched on-chip communication. Conventional computer design tools i.e. Network Simulator-2 utility are used for network design and simulation. It provides a versatile practice and visualization environment for the design, configuration, and troubleshooting of network environments. The work done by us uses same tool to compare two topologies. The 2-D mesh is currently the most popular regular topology used for on-chip networks in tile-based architectures, because it perfectly matches the 2-D silicon surface and is easy to implement. However, a number of limitations have been proved in the open literature, especially for long distance traffic. In this type of topology, every node has a dedicated point to point link to every other node in the network. This means each link carries traffic only between the two nodes it connects. If N is total no of nodes in network. Number of links to connect these nodes in mesh & DPS = N (N-1)/2 Each node should have (N-1) I/O ports as it require connection to every another node. The advantages are:
- No traffic problem as there are dedicated links. Robust as failure of one link does not affect the entire system.
- Security as data travels along a dedicated line.
-Points to point links make fault identification easy.
 Disadvantages are:
-The hardware is expansive as there is dedicated link for any two nodes and each device should have (N-1) I/O ports.
- There is mesh of wiring which can be difficult to manage.
- Installation is complex as each node is connected to every node. Also in DPS topology Figure 1(b) shows a diagram of a scaled down 4x4 grid with a similar organization. One column in the middle of the grid is devoted to shared resources

with one terminal per node; the rest of the network employs 4- way concentration.
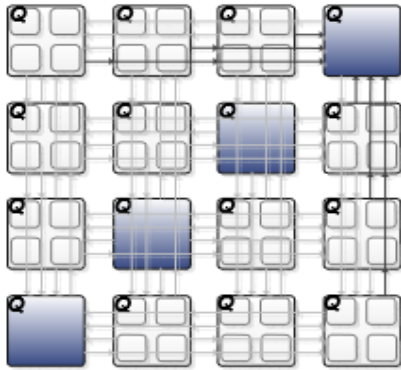
(a) Baseline QOS –enabled approach
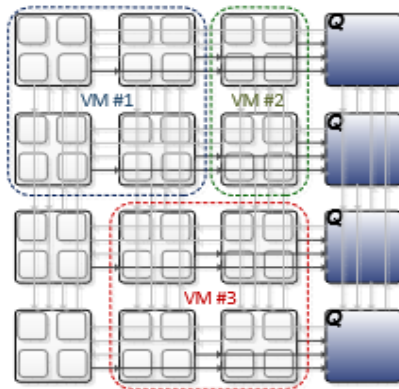
a)Topology Aware QOS Approach

As earlier studies have shown that maximum power is consumed by links and interconnect infrastructure. Reducing interconnects and links will result in lower power consumption but can also affect the performance and reliability negatively. The topology suggested by us reduces the number of links thus resulting into lower power consumption keeping same level of reliability and performance level

IV   SIMULATION

Network Simulator Ns-2 The simulator, ns-2, has facilities to describe network topology, network protocols, routing algorithms and communication traffic generation. It provides basic TCP and UDP as the network transmission protocols, four routing strategies (Static, Session, Dynamic and Manual) and many mechanisms for modelling traffic generation. It is possible to generate a traffic at random, by burst or with bias towards destinations. Additionally, the simulator has the possibility of incorporating protocols, routing algorithms and traffic generation defined by the user. The simulator is written in C++ and uses OTcl (Object Tool Command Language) for building command and configuration interfaces. The source code of ns-2 is also available[5]. Ns-2 provides well documented trace format for interpreting simulation results. A graphical animator tool, nam (Network AniMator), is also built into ns-2 for user's friendly visualization of the flow of messages and the whole system simulated. In this paper, a generic NOC architecture would be modelled and simulated in ns-2 with only built-in options. Tcl is used for specifying the NOC simulation model and running the simulation.

V CONCLUSION

The results achieved in terms of time and reduction in number of links displayed here is encouraging and motivates us to take the work further. As discussed earlier the NoC technology can borrow the tools and techniques from conventional computer network technology with required customization. In our future work, we intend to test same on a standard NoC benchmark. The other design parameters on NoC will also be explored.

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SPECKLE NOISE REDUCTION FILTERS ANALYSIS

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Abstract— Speckle noise reduction from echocardiographic images is essential to study them for medical analysis point of view. But it has been remain a challenging task for the medical world. Speckle noise gets introduced to them at the time of acquiring such images and also due to the nature of acquiring system. To reduce the speckle noise from echo images image processing filters such as Median, Lee, Frost, Kuan, Enhanced Lee and Frost, Weiner, Gamma Map are used. But they have different behavior on different variance of the speckle noise. This paper is the analysis of above mentioned filters with quality metrics against speckle variance. Quality metrics used are SNR, PSNR, ASNR, FOM, CNR, SSIM, MSE.

Index Terms— Echocardiographic Images, Speckle Noise, Speckle Filters, SNR, PSNR, APSRR, FOM, SSIM, CNR, MSE.

I. INTRODUCTION

Echocardiographic and ultrasound images are usually noisy images. As they are taken from far distance or from far internal organs of body as heart, brain, kidneys etc. Hence they get corrupted because of speckle noise. Speckle noise has granular pattern and it is tedious to remove. Classical filters give more accurate reduction of noise from echo images [1].

Two basic models of noise are Additive and Multiplicative. Additive noise is systematic and can be modelled, hence can be removed easily but multiplicative noise is image dependent, it is hard to model and hence cannot be removed easily. When the multiplicative noise is generated due to de-phased echoes it is called as Speckle noise. Speckle is the result of diffuse scattering [2]. Speckle noise has standard variance of 0.04 and as it increases speckle noise also increases [3]. Hence filters behave differently for different variance factor. Mathematically speckle noise can be modelled as in eqn. (1) [4]. Where $g(m,n)$ is image with noise, $u(m,n)$ is multiplicative component and $\eta(m,n)$ is the additive component of speckle noise.

$$g(m,n) = f(m,n) * u(m,n) + \eta(m,n) \qquad (1)$$

This work gives the analysis of such filters over different variance with the qualitative measurement of quality metrics such as SNR, PSNR, ASNR, FOM, CNR, SSIM, MSE [1]. In this work eight filters and seven different quality metrics are used for five variance values. This work is arranged in the paper as following. Section II describes algorithms for speckle filters. Section III contains quality metrics details. Section IV discusses on the result analysis and section V concludes the discussion.

II. SPECKLE FILTERS

Basically speckle filters can be classified as scalar (mean and median) and adaptive filters (Lee, Frost, Kuan etc). Both types of filter use a moving window [5]. The main difference between them is that the adaptive filters usually include a multiplicative model and the use of the

local statistics. The Frost filter is an adaptive filter, and convolves the pixel values within a fixed size window with an adaptive exponential impulse response. The Lee filter performs a linear combination of the observed intensity and the local average intensity value within the fixed window [6]. In this section some of them are explained with their respective algorithms.

A. Median Filter

In median filter operation centre pixel is replaced by the median value of all pixels and hence produces less blurring and it preserves the edges.

Algorithm: 1. Take a 3×3 (or 5×5 etc.) region cantered around the pixel (i, j).

2. Sort the intensity values of the pixels in the region into ascending order.

3. Select the middle value as the new value of pixel (i, j).

B. Frost Filter

The Frost filter reduces speckle noise and preserves important image features at the edges.

Algorithm: $K = e^{(-B * S)}$

Where $B = D * (L_V / L_M * L_M)$

S : Absolute value of the pixel distance from the centre pixel to its neighbors in the filter window

D : Exponential damping factor (input parameter),

L_M : Local mean of filter window

L_V : Local variance of filter window.

The resulting gray-level value of the filtered pixel is

R = (P1 * K1 + P2 * K2 + ... + Pn * Kn) / (K1 + K2 + .. + Kn)

Where P1,P2,...Pn are gray levels of each pixel in the filter window. K1,K2,...Kn are weights (as defined above) for each pixel.

C. Lee Filter

This filter reduces speckle noise by applying spatial filter to each pixel.

Algorithm: $L_M + K * (P_C - M * L_M)$

Where, K(weighting function)$= M * L_V / ((L_M * L_M * MV)(M * M * L_V))$

Where $MV = 1/NLooks$

P_C : Centre pixel value of window

L_M : Local mean of filter window

L_V : Local variance of filter window

M : Multiplicative noise mean (input parameter)

MV : Multiplicative noise variance (input parameter)

Nlooks : Number of looks (input parameter)

D. Weiner Filter

It reduces noise from image by comparing desired noiseless image. Weiner filter works on the basis of computation of local image variance.

$$f(u,v) = \left[\frac{H(u,v)^*}{H(u,v)^2 + \left[\frac{Sn(u,v)}{Sf(u,v)}\right]} \right] G(u,v)$$

Where, $H(u,v)$ = Degradation function

$G(u,v)$ = Degraded image

$Sn(u,v)$ = Power spectra of noise

$Sf(u,v)$ = Power spectra of original image.

E. Kuan Filter

Applies a spatial filter to each pixel in an image, filtering the data based on local statistics of the centered pixel value.

Algorithm: The resulting filtered pixel value is:

R = P_C * K + L_M * (1 - K)

Where, C_U = 1 / sqrt (NLooks) : Noise variation coefficient

C_I = sqrt (L_V) / L_M : Image variation coefficient

K = (1 - ((C_U * C_U) / (C_I * C_I))) / (1 + (C_U * C_U))

P_C : Centre pixel value of window

L_M : Local mean of filter window

L_V : Local variance of filter window

Nlooks : Number of looks

F. Enhanced Lee Filter

The enhanced Lee filter is an altered version of the Lee filter reducing the speckle noise effectively by preserving image sharpness and detail.

Algorithm: Value of smoothed centre pixel:L_M for $C_I <= C_U$

L_M * K + P_C * (1 - K) for $C_U < C_I < C_{max}$

P_C for $C_I >= C_{max}$

where P_C : Center pixel value of window

L_M : Local mean of filter window

SD : Standard deviation in filter window

Nlooks : Number of looks (input parameter)

D : Damping factor (input parameter)

C_U = 1 / square root (NLooks)(Noise variation coef.)

C_{max}=srt(1+2/NLooks)(Max.noise variation coef.)

C_I = SD / L_M(Image variation coefficient)

$K = e^{(- D (C_i - C_U) / (C_{max} - C_I))}$

G. Enhanced Frost Filter

Algorithm: $W(x,y) = e^{-kfunc(C_I(x',y'))|(x,y)|}$

Where $func(C_I(x',y'))$ is a hyperbolic function of $C_I(x',y')$ defined as follows.

$$func(C_I) = \begin{cases} 0 & for\ C_I(x',y') < C_B \\ \frac{[C_I(x',y'-C_B]}{[C_{max}-C_I(x',y')]} & for C_B \le C_I(x',y') \le C_{max} \\ \infty & for\ C_I(x',y') > C_{max} \end{cases}$$

H. Gamma Map Filter

Based on the application of maximum a posteriori (MAP) approach, which required the a priori knowledge of the probability density function (PDF) of the image.

Algorithm:

$$U(x',y') = \begin{cases} I'(x',y') & C_I(x',y') < C_B \\ \frac{(\alpha-L-1)(x',y')+\sqrt{I^2(x',y')(\alpha-L-1)+4\alpha LI'(x',y')}}{[C_{max}-C_I(x',y')]} & for C_B \le C_I(x',y') \le C_{max} \\ I(x',y') & for\ C_I(x',y') > C_{max} \end{cases}$$

Where L is the number of looks,

$C_{max}(x',y') = \sqrt{2C_B}$

And $\alpha = \frac{1+C_B^2}{C_I^2(x',y')-C_B^2}$

III. QUALITY METRICS

For the quantitative assessment seven quality metrics are used on both noisy and filtered images. Quality metrics that are used in this work are signal to noise ratio (SNR), peak signal-to-noise ratio (PSNR), average peak signal-to-noise ratio (APSNR), Pratt's figure of merit (FoM), contrast-to-noise ratio (CNR), structural similarity (SSIM), edge-region mean square error (MSE). These are explained in following sections.

A. SNR

This is fundamental parameter to measure level of noise. It is widely used. It is the ratio of mean to the standard deviation of pixel amplitudes in an image. Image having maximum speckle noise has SNR 1.91. There is indirect proportion between speckle noise and SNR [14].

$$SNR = 10 \log_{10} \frac{\sigma_g^2}{\sigma_e^2}$$

B. PSNR:

PSNR is defined from RMSE and quantifies the ratio between the possible power of a signal and the power of corrupting noise [15]. For a gray level image with 256 gray levels, PSNR is defined as,

$$PSNR = 20log_{10}(\frac{255}{RMSE})$$

Where, $RMSE = \sqrt{MSE}$

$$MSE(I_{filt},I_{ref}) = \frac{1}{XY}\sum_{i=1}^{Y}\sum_{j=1}^{X}(I_{filt}(i,j) - I_{ref}(i,j))^2$$

C. APSNR:

A simple average of PSNR per frame is called APSNR [15]

D. FOM:

FoM is an estimator for quantifying the edge pixel displacement between the edge masks of filtered and reference images, and is defined as [16],

$$FoM(I_{filt},I_{ref}) = \frac{1}{max(N_{filt},N_{ref})}\sum_{i=1}^{N}\frac{1}{1+d_i^2\alpha}$$

Where, di = Euclidean distance between the ith detected edge pixel and the nearest original edge pixel, and

α = constant and set to 0.1

E. CNR

This metric operates on a single image and exploits levels of contrast between two different regions of images [8]. One region is a region of interest (ROI) and the other can be a part of the background. This metric is calculated as

$$CNR = \frac{|\mu 1-\mu 2|}{\sqrt{\sigma 1^2+\sigma 2^2}}$$

Where, $\mu 1$ and $\sigma 1$ are mean and variance of ROI and $\mu 2$ and $\sigma 2$ are mean and variance of background.

F. SSIM:

Index is another metric for measuring the similarity between two images. This metric has much better consistency with the qualitative appearance of the image [1].

$SSIM$

$$= \frac{1}{M} \sum \frac{(2\mu 1 \mu 2 + C1)(2\sigma_{1,2} + C_2)}{(\mu_1{}^2 + \mu_2{}^2 + C_1)(\sigma_1{}^2 + \sigma_2{}^2 + C_2)}$$

Where, $\mu 1$ and $\mu 2$ are the means and and $\sigma 1$ and $\sigma 2$ are the standard deviations of the images being compared. $\sigma_{1,2}$ is the covariance between them. SSIM has value between 0 and 1, when it is equal to 1 images are structurally equal.

G. MSE:

This measures the average absolute difference between two images [17].

$$MSE\big(IE_{filt}, IE_{ref}\big) =$$

$$\frac{1}{XY} \sum_{i=1}^{Y} \sum_{j=1}^{X} \Big(IE_{filt}(i,j) - (i,j)\Big)^2$$

Where IE_{filt} and IE_{ref} are edges of filtered and reference images respectively. The edge-region MSE measures the average differences in edge regions.
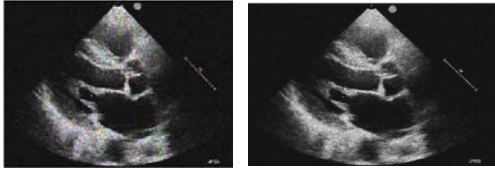
Fig. (a) noisy image   Fig. (b) Lee Filtered Image
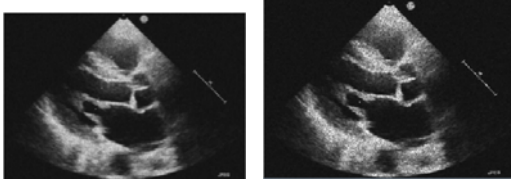
Fig. (c) Frost Filtered Image   Fig. (d) Weiner Filtered Image
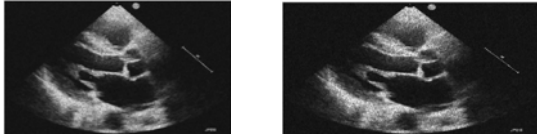
Fig.(e) Mean Filtered Image Fig.(f) Median Filtered Image
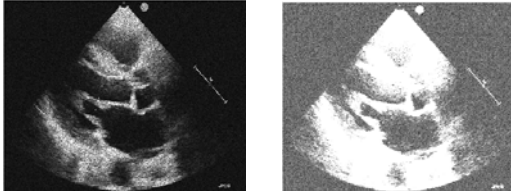
Fig.(e)Adv. Lee Filtered Image   Fig.(f) Adv. Frost Filtered Image
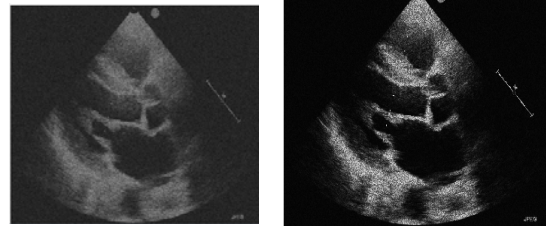
Fig.(e) Kuan Filtered Image Fig.(f) Gamma Map Filtered Image

IV. EXPERIMENTAL RESULTS AND ANALYSIS

To remove speckle noise from echo images nine filters (Lee, Frost, Mean, Median, Kuan, Advanced Lee and Frost, Gamma Map and Wiener) are used in this work. This filtering is done for five values of variances (0.02, 0.04, 0.06, 0.08 and 0.1). Results are shown in following figures. Figure (a) is noisy image having variance 0.08. Figures (b) to (j) are filtered images.

Result analysis is done by measuring seven quality metrics (SNR, PSNR, ASNR, FOM, CNR, SSIM, MSE.) Following tables shows comparative analysis of nine filters for five different variance value.

V. CONCLUSION

This work filters the speckle noise with the help of nine different filters. Filtering analysis is done by using the seven different quality metrics for five variance values. As speckle variance increases noise also increases. For higher values of speckle variance filter performance reduces slightly. In tables bold value shows the more correct value for that variance. Adaptive filters such as Lee, Frost, Advanced Lee and Frost and wiener gives more appropriate results.

Table 1. Quality metrics readings for speckle variance 0.02

Quality Metrics	SNR	PSNR	ASNR	FOM	CNR	SSIM	MSE
Mean	14.06	22.71	0.055	0.13	0.04	0.73	635.7
Median	17.15	25.69	**0.03**	0.14	0.02	0.74	222.1
Lee	**18.59**	**26.08**	0.031	0.13	0.02	**0.77**	211.3
Frost	17.15	24.72	0.32	**0.18**	0.02	0.74	279.4

	SNR	PSNR	ASNR	FOM	CNR	SSIM	MSE
Kuan	6.17	14.68	0.36	0.13	0.33	0.6	3688
Adv. Lee	17.15	25.04	0.031	0.11	0.02	0.73	234.1
Adv. Frost	0.032	6.43	1.42	0.06	**1.42**	0.04	1887
Wiener	18.58	26.19	0.031	0.11	0.02	**0.77**	**178.5**
GMap	0.032	6.43	1.43	0.08	1.4	0.04	1909

Table 2. Quality metrics readings for speckle variance 0.04

	SNR	PSNR	ASNR	FOM	CNR	SSIM	MSE
Mean	13.61	22.2	0.07	0.13	0.05	0.69	700.6
Median	15.6	24.17	**0.042**	0.14	0.02	0.68	307.8
Lee	**17.31**	**24.98**	0.05	0.13	0.03	**0.73**	**279.4**
Frost	16.41	24.19	0.05	**0.17**	0.02	0.71	330.2
Kuan	6.009	14.52	0.37	0.13	0.34	0.54	3813
Adv. Lee	13.96	22	0.05	0.12	0.02	0.64	469.2
Adv. Frost	0.032	6.429	1.42	0.06	1.42	0.04	1889
Wiener	15.76	23.69	0.05	0.11	0.02	0.70	314.5
GMap	0.032	6.429	1.43	0.07	**1.43**	0.04	1909

Table 3. Quality metrics readings for speckle variance 0.06

Quality Metrics	SNR	PSNR	ASNR	FOM	CNR	SSIM	MSE
Mean	13.22	21.78	0.08	0.13	0.06	0.67	766.7
Median	14.48	23.09	**0.05**	0.13	0.04	0.65	392.4
Lee	**16.36**	**24.19**	0.06	0.13	0.04	**0.70**	**348.7**
Frost	15.9	23.71	0.06	**0.18**	0.04	**0.70**	383.8
Kuan	5.843	14.38	0.38	0.13	0.35	0.50	3924
Adv. Lee	12.7	20.19	0.06	0.10	0.04	0.58	712.5
Adv. Frost	0.032	6.429	1.42	0.08	1.42	0.04	1889
Wiener	14.02	22.08	0.06	0.10	0.04	0.66	457.9
GMap	0.032	6.429	1.43	0.06	1.43	0.04	1909

Table 4. Quality metrics readings for speckle variance 0.08

Quality Metrics	SNR	PSNR	ASNR	FOM	CNR	SSIM	MSE
Mean	12.81	21.37	0.09	0.13	0.07	0.65	844.1
Median	13.58	22.22	**0.06**	0.12	0.04	0.62	482.7
Lee	**15.47**	**23.38**	0.07	0.13	0.05	**0.68**	**424**
Frost	15.31	23.26	0.07	0.15	0.05	**0.68**	443
Kuan	5.62	14.22	0.38	0.13	0.36	0.47	4035
Adv. Lee	10.73	18.9	0.07	0.10	0.05	0.53	964.2
Adv. Frost	0.030	6.429	1.42	**0.16**	1.42	0.04	1889
Wiener	12.71	20.89	0.07	0.11	0.05	0.62	608.2
GMap	0.030	6.429	1.43	0.06	**1.43**	0.04	1909

Table 5. Quality metrics readings for speckle variance 0.1

Quality Metrics	SNR	PSNR	ASNR	FOM	CNR	SSIM	MSE
Mean	12.44	20.95	0.10	0.12	0.08	0.63	911.5
Median	12.97	21.52	**0.06**	0.12	0.05	0.59	563.1
Lee	14.8	22.77	0.07	0.14	0.05	0.66	494.1
Frost	**14.86**	**22.86**	0.07	0.15	0.06	**0.67**	498.4
Kuan	5.56	14.11	0.38	0.13	0.36	0.44	4133
Adv. Lee	9.73	17.9	0.07	0.10	0.06	0.49	1209
Adv. Frost	0.03	6.429	1.42	**0.18**	1.42	0.04	1889
Wiener	11.74	19.95	0.07	0.11	0.06	0.59	**755.4**
GMap	0.03	6.429	1.43	0.06	**1.43**	0.04	1909

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TEXT-TO-SPEECH SYSTEM FOR GUJARATI LANGUAGE

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Abstract—— In this paper we describe Speech synthesis which also called as Text – to-speech synthesis. The speech synthesized is the artificial generation of human speech from text (Gujarati text). The required database in the conversion of character-to-sound is recorded by PRAAT software and is saved in .wav format in the directory. The smallest segment of the recorded voice is concatenated to produce speech of the desired words. The main aim of using this method is, it is simple. Concatenation technique is used and software used is MATLAB.

Keywords—*Concatenative synthesis, gujarati, praat, tts, unicode, PESQ.*

I. INTRODUCTION

The word 'Synthesis' is defined by the Dictionary as 'the putting together of parts or elements so as to form a whole'. Speech synthesis generally refers to the artificial generation of human voice – either in the form of speech or in other forms such as a song. The computer system used for speech synthesis is known as a speech synthesizer. There are several types of speech synthesizers (both hardware based and software based) with different underlying technologies. For example, a TTS (Text to Speech) system converts normal language text into human speech, while there are other systems that can convert phonetic transcriptions into speech. The basic principle behind speech synthesis is known as the source-filter theory of speech production – that

is, the information about the voice source and the vocal tract filter can be separated from each other.
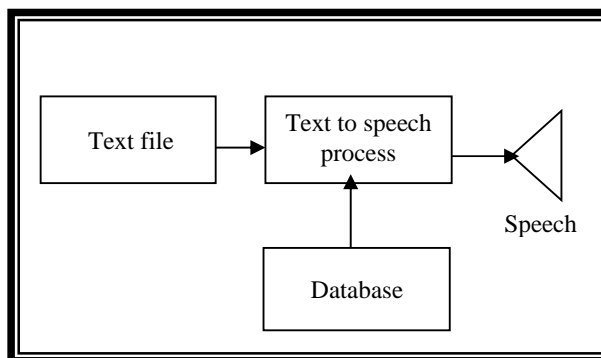
Fig. 1. *Block diagram of normal text-to-speech system.*

Today, speech synthesizers are a common feature in most operating systems. Speech synthesis applications have also made computing related services more inclusive by allowing access to people with visual impairments or reading disabilities.

The quality of a speech synthesizer is measured based on two primary factors – its similarity to normal human speech (naturalness) and its intelligibility (ease of understanding by the listener). Ideally, a speech synthesizer should be both natural and intelligible, and speech synthesis systems always attempt to maximize both characteristics. Evaluation of speech is done through MOS mainly, but in this paper evaluation of speech is planned with PESQ method.

II. OVERVIEW OF GUJARATI LANGUAGE

Gujarati (ગુજરાતી) is an Indo-Aryan language native to the West Indian region of Gujarat. The Gujarati script was adapted from the Devanagari script to write the Gujarati language. It is part of the greater Indo-European language family. Gujarati is descended from Old Gujarati. Gujarati is a modern IA (Indo-Aryan) language evolved from Sanskrit.

In Guajarati language there are 33 consonants and 13 vowels. The phonemes are divided into two type's vowels (swaras) and consonants (vyanjanas).

vowels (swaras): Vowels are the independently existing letters. Vowels sound cannot be modified.

V VF > . p µ k VV{ VM VF{ V\ Vo

Consonants (vyanjanas): Consonants are those which are depend on vowels to form their independent letters. The sound of the consonant can be modified by combining vowels with them.

SBU3RKHh 890-6TYN WG5OAEDI
Z,JXQF;C/   1F7

III. SYNTHESIZER TECHNOLOGY USED

A. Concatenative Synthesis

Concatenation is also called as cut and paste synthesis in which short segment of speech are selected from a pre-recorded database and joined one after another to produce the desired utterance. In this the quality of speech is high but there many b some limitation due to the memory capacity. The longer selected units are the fewer problematic concatenation point will occur in the synthesis speech, but at the same time memory requirement increases. The length of unit selections can be phonemes and diaphones because they are short enough to attain sufficient flexibility and to keep the memory requirement reasonable. Their use of provide good quality speech to take account of co-articulation cause they contain third transition from one phonemes to another and later half of the later phonemes. The use of phonemes is the most flexible way of generating various utterances.[6]

In phonemes and diaphone concatenation is the greatest challenge in the continuity and to avoid audible distortion caused by the difference between successive segments, at least the fundament frequency and the intensity of the segment must b controlled. It is a troublesome process of creating the database from which unit be selected. [2][3]

IV. CREATION OF DATABASE

For Gujarati language there are 426 phonemes including vowels and consonant and their combination. The combination include here is C, CV, V, VC where C is the consonant and V is the vowel. The algorithm used to merge the characters or word is concatenation method. The entire 426 phonemes database is created in the form of wave files (.wav) by using PRAAT software and Fs is 44100 Hz Where 13 phonemes are vowels and 34 phonemes are consonant and rest are their combinations.

TABLE 1. *Phonemes along with the letters with examples (Gujarati)*

Sr. no	Phonemes	Example
1.	SF	SFSF
2.	9	9l/IM
3.	,L	S,L

TABLE 2. *Examples of all possible combinations of 'S'.*

Sr. no	Phonemes combinations
1.	S + V = S
2.	S + VF = SF
3.	S + > = IS
4.	S + . = SL
5.	S + p = S]
6.	S + µ = S}
7.	S + k = S=
8.	S + V[= S[
9.	S + V{ = S{
10.	S + VM = SM
11.	S + VF{ = SF{
12.	S + V\ = S\

A. FOR GUJARATI LANGUAGE

The process of transformation from text to speech contains mainly two phrases.

- The text analysis,

- Then the resulting information is used to generate the speech signal (speech synthesis).
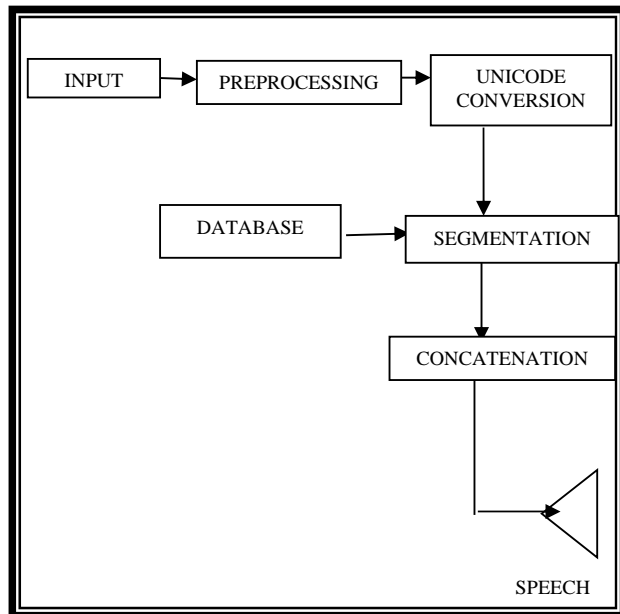
Fig. 2. *Block diagram for TTS for Gujarati language.*

Text analysis means syntactic and semantic analysis is done and to identity the font in which the given text is encoded and applying the Unicode to given font is done in Unicode conversion and the phonetic analysis is done in this which the graphemes are converted into phonemes. Then prosodic analysis in which pitch and duration attachment is occurred. Then finally speech synthesis in voice rendering is done and that sound is produced. The pre-recorded phonemes are concatenated according to the given text characters.
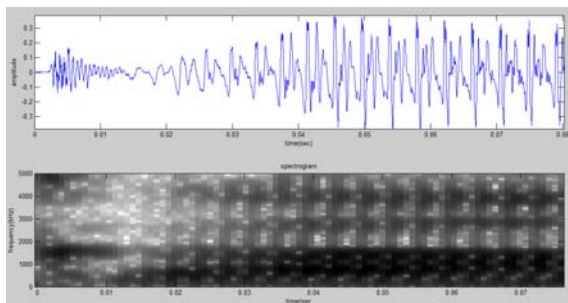
Fig. 3. *Output of speech "S"*
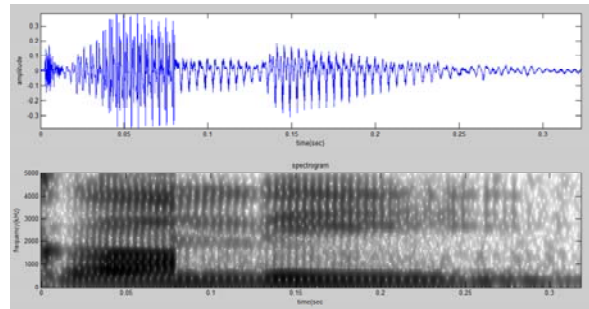
Fig. 4. *Output of speech "S,L"*
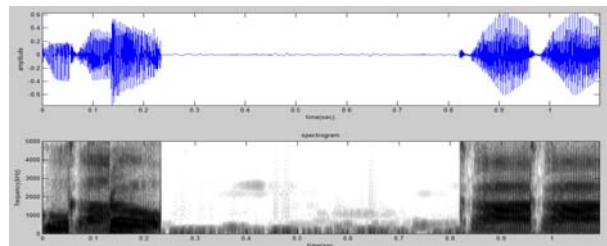
Fig. 5. *Output of speech "S}S0M SFSF".*
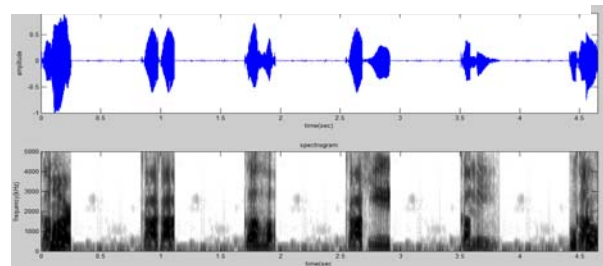
Fig. 6. *Output of speech "SD/ SFSF So SFSL S,L S}S0M".*

VI. QUALITY TEST

To measure the speech quality there are two approaches: subjective and objective. The subjective listening tests a subject hears a recorded speech of a processed voice file and the quality using an opinion scale and the MOS is then calculated as an average of participant scores. Objective models have been developed to provide machine-based automatic assessment of the speech quality score. The measure is derived from the input text and the natural speech corpus and is inversely proportional to the overall speech quality-the higher number of concatenations, the lower is the quality. Alternatively, signals based measures have been proposed which focus on the computing spectral distances between the target synthesized speech signal and its original natural speech.

Since perceptual evaluation of speech quality(PESQ) is a more popular tool and has been widely deployed in the industry and many

research area and is composed of five scores of objective quality.

TABLE 3. *Score of objective listening test*

rating	Description
5	Very natural, no degradation
4	Fairly natural , little degradation
3	Somewhat natural, somewhat degraded
2	Fairly unnatural, fairly degraded
1	Fully unnaturally, fully degraded

TABLE 4. *Objective listening test results.*

Test set	PESQ
SFSF	4.14
So	4.35
SD/	3.36
9I/IM	3.914
RS,L	4.681
S\SI	2.627

VII. CONCLUSION

This paper discusses the design and development of Gujarati text to speech for concatenation based TTS system. This paper have selected C,CV,V,VC patterns only. Since this method is very easy and efficient to implement as compared with other methods. And can conclude that the speech produced is preserving naturalness and good quality based on the objective quality test results. This can be applied for different languages with more naturalists in them. As future work can b apply on word documents, and with advanced version can apply on PDF, scanned data etc. by some modifications.

Acknowledgment

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AN APPLICATION OF DENOISING METHODS FOR VIDEO COMMUNICATION

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Abstract—High Efficiency Video Coding (HEVC) which is a new video standard is decided freshly. HEVC increases the video coding rate performance, but the difficulty in coding also increases in association with the old standards. In very professional applications of video domain compression perfor-mance is controlled by noise. So it is essential to analyze the denoising performance in high efficiency video. The performance of quantization parameters from low to medium is present and noise due to source is present in the reconstructed frames. This is unambiguous in-loop frame denoising filter for this range. The noise which was badly influences the prediction can be modeled and estimated by using methods discussed in the paper. The denoising filter which exploits the HEVC core transform is discussed. A coding mode adaptive arrangement for motion compensation with noise filtered reference frame is discussed and described. The compression will indicate that especially for low to medium quantization parameters, settings for lossless compression noticeably bit-rate savings and it can be manipulated.

Index Terms—Video enhancement; Noise reduction techniques in Video; Video denoising; Video compression; Video communi-cation

I. INTRODUCTION

Input video sequences of a video encoder can be desta-bilized due to different noise sources. One of key sources of impurity for video sequences is the additive noise intro-duced by the video camera or similar device. Analog video signals are frequently degraded due to channel noise in the conventional analog transmission systems. These are essential to be sometimes digitally converted in the receiver side. Many analog video applications such as DVD recorder can encode analog video signals, e.g., NTSC/PAL. Though, noisy analog video signals are not only visually irritating, but they are also tough to be encoded competently owing to uncorrelated nature of noise. There are many noise reduction techniques for video sequences is available. A spatial-domain adaptive filtering system and a motion-compensated spatio-temporal filtering system have decent de-noising performance. The conventional denoising schemes have been devised in the light of noise reduction itself rather than optimal combination of filtering with a video encoder. The noise reduction operation is independent of video encoding. Transform-domain Wiener filtering achieves fast denoising because all the processing is worked in the DCT domain simply by mounting the DCT coefficients.
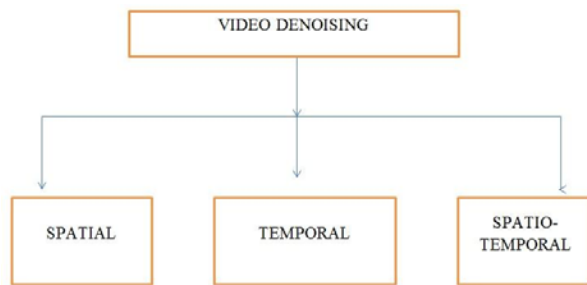
II. VIDEO DENOISING METHODS

Fig. 1. Video denoising methods.

Video is made up of temporal combination if many images spacing at little time distance. so when the video is comprising of noisy content it should be processed. Video enhancement and noise reduction has been one of the popular research area.the main objective of video denoising algorithms is that removal of the noisy content without altering the original video. When including the denoising difficulty from image information to video information, temporal correlation of noisy content is considered as first priority. [1] suggested a method of temporal filtering to noise suppression with preserving image edges at the same time. These temporal filtering methods were based on block motion estimation. In [2] applied the KarhunenLoeve (KL) transform alongwith the temporal direction to decorrelate dependency amongst successive frames and then used adaptive Wiener filtering to flat frames. Maximum methods using temporal filtering work sound for still or slow-motion video subsequently temporal filtering can be done attractively with exact motion evidences. Huge motion estimation incorrectness occurring in fast motion video has a tendency to result in inaccurate noise estimation, as it demands for a vast memory buffer to apply temporal filtering.
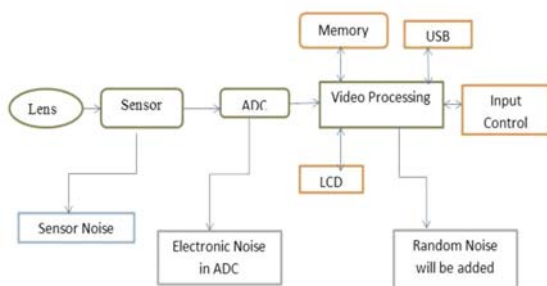
Fig. 2. Sources of noise in video.

III. RELATED WORK

In [3] discussed a technique for film grain noise extraction, modeling and synthesis is calculated and applied to high-definition video coding. Film grain noise improves the natural appearance of pictures in high-definition video and should be conserved in coded video. The coding of video information with film grain noise is costly. It was proposed to enhance the coding performance by removing film grain noise from the input video at the encoder before the main processing step, and again combining it back to the decoded video at the decoder processing step. Implementing this method, with removing film grain noise from image or video with a varying denoising method without changing its original information is important. Execution of a parameter based prototype to generate film grain noise that is close to the real one is essential. This can be done with observed characteristics i.e. power spectral density and the cross channel spectral correlation. Using this framework, the coding gain of denoised video is higher although the visual quality of the concluding reconstructed video is well conserved.

The total variation minimization method is used for noise reduction purpose, to conquer film grain noise. Denoising tech-nique influence distortion zones which have sharp conversion between neighboring pixels, it is very much significant to recognize areas of image edges before applying the denoising process. In smooth areas performance of denoising will be selectively only. The denoising method based on the total variation minimization standard can be of more comprehensive with some prior data of noise. The preprocessing task at the encoder can be divided into three steps

1)Temporal information is used to extract noise character-istics

2)Identify smooth regions of the image

3)Prior noise information is used to denoise each image.

In [4] proposed a technique of film grain noise which is inherent in analog film stock and is generated in the process of exposing and developing silver-halide crystals. Film grain noise can be modeled as a zero-mean Gaussian noise and the noise variance varies with the intensity of noise-free signal. Film grain noise is

temporally independent. Film grain noise is spatially correlated. The higher the image resolution is, the more likely that the viewer will perceive the film grain noise. For high-definition videos, the film grain noise is significantly noticeable, which is the essential part of the original of the video, thus, it is desired to maintain in the encoded video. However, the encoding of film grain noise pays a lot because of its random characteristics. Since the film grain noise is temporally independent, it can not be predicted by motion compensation. As a consequence, most of the film grain noise remains in the prediction residue, and it costs many bits to encode in the DCT domain because the film grain noise contains a lot of high-frequency components.

In addition, the existence of film grain noise has an adverse influence on the accuracy of motion estimation, which further reduces the coding efficiency. To overcome those problems mentioned above, first propose the film grain noise encoding structure described in [5], in which film grain noise is detached from the original video sequence as the pre-processing step and encoded as a parameterized example. and then the decoder simulates the film grain noise based on the transmitted model parameters. Old method not provide any specific method to estimate the noise parameters or any method to remove the film grain noise, and these methods will be explored in our work. [6] propose that the H.264/MPEG-4 AVC encoder itself is used as the film grain elimination filter and the film grain noise is evaluated by subtracting the encoded picture from the original picture; then, only one representative macroblock of film grain is encoded and transmitted, and the film grain noise for the whole frame is obtained by mirroring, rotation and scaling the encoded macroblock of film grain. The appearances of film grain noise for different macroblocks can differ a lot, thus it is hard and unreasonable to find a demonstrative macroblock of film grain. The film grain noise found also consists of coding artifacts, which are spatially variant. In image edges are first checked and a 2D spatial filtering operation is applied to remove film grain noise in non-edge areas while edge regions are kept as original.

The coding efficiency is considerably

amplified because the noise is partially removed. There is still chance for improvement. Since spatial filtering is used for denoising, to avoid distortion and blur, only the noise in non-edge regions is filtered. So for video containing full of edges, the increase of coding efficiency will be restricted. The spatial filtering does not reflect the signal dependent characteristics of the variance of film grain noise. First, based on the features of film grain noise, the spatial correlation of noise and the relationship between noise variance and signal intensity are estimated. Then, to avoid the blurring problem and to fully utilize the temporal correlation of video sequence, a temporal filter based on multi assumption motion compensation is used for extracting the film grain noise. Finally, the film grain noise is modeled and synthesized by an AR model.

IV. UNDERSTANDING FROM EXISTING METHODS

The main disadvantages of video denoising algorithms are as follows

TABLE I
COMPARISON OF ALGORITHMS

Algorithm	Method	Step	Type of filter
Film grain noise extraction	Pre-processing Step	Smooth Region Detection and Denoising	Nonlinear Filtering Approach
Film grain noise removal	Pre-processing step		Multi-Hypothesis Motion Compensated Filter
In-Loop Denoising For Lossless Coding	In Loop	Denoising of reference frame	Adaptive Wiener Filter
Non-Local In-Loop Denoising	In Loop	Denoising of reference frame	low complexity adaptive Wiener filter,and the BM3D algorithm
In The Loop Denoising Filter For Impulse Noise Reduction	In Loop	Impulse Noise Reduction	Adaptive Median Filter
HEVC Deblocking Filter	In Loop	Reduce visible artifacts at block boundaries	deblocking filter
Loop filter for Motion Compensated Frame	loop filter	Motion compensated frame	Adaptive Loop filter and adaptive interpolation filter

1)   The number of skipped blocks increases with increasing QP, the complexity of framework becomes relatively high with increasing QPs compared with the unmodified HEVC.

2)   Increasing the sliding step size also reduces the effi-ciency of the FDF-based algorithms.

3)   For example, using a sliding step size of two reduces the complexity by a factor of four and at the same time also the average bitrate savings are reduced by approximately 2%.

4)   Together with the noise estimation process, the complex-ity of the whole in-loop denoising framework is approx-imately twice the complexity of the interpolation filter, which is especially visible for high QPs in which the motion compensation process dominates the decoding complexity.

5)   The introduced reference frame denoising scheme is not very efficient for high QPs and could therefore be switched off.

6)   For low QPs, where the introduced framework is effi-cient the additional complexity in the decoder is rela-tively small. The reason for this behavior is that more processing in the decoder is required using low QPs because less SKIP modes are used

V. COMPARISON OF ALGORITHMS

Most methods using temporal filtering work well for still or slow-motion video since temporal filtering can be done nicely with accurate motion information. However, large motion estimation errors occurring in fast motion video tend to result in erroneous noise estimation. Furthermore, it demands a large memory buffer to implement temporal filtering.

1)   Spatial video denoising method where image noise re-duction is applied to each frame individually

2)   Temporal video denoising methods ,where noise be-tween frames is reduced. Motion compensation may be used to avoid ghosting artifacts when blending together pixel from several frames.

3)   Spatial-Temporal video denoising methods use a com-bination of spatial and temporal denoising this is often referred to as 3D denoising

VI. CONCLUSIONS

As in different applications preprocessing cannot be applied. Other possibilities for coding of noisy video content have to be considered. Therefore, the inter-frame prediction within a video codec is analyzed by In-Loop Filtering algorithm. It has been motivated that an in-loop denoising framework can be established for efficient coding of noisy video content. It has been shown that noise is still present for a wide range of QPs. Different denoising techniques are studied in this work, which is applied for improving of noisy video content.

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A METHOD FOR DISTRIBUTED REAL TIME AGGREGATIONS

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Abstrac—This paper focuses on various approaches and proposes a method for aggregations in distributed environment and its importance for analysing the data. Aggregation operations are the most used operations in the analysis of big data. Traditionally data collected over a period of time was analysed by storing it in the data-warehouse or database with the help of aggregation operations. This paper mainly focuses on the various aggregation operations and their use in business analytics and also the significance and role of distributed computing to perform these aggregations in real time to analyse continuously streaming data to get analysis results in the real time and improve the decision making.

Index Terms— Real-Time Aggregations, Distributed Computing, Analytics, AKKA Actors, KPI's(key performance Indicators)

I. INTRODUCTION

OLAP (Online Analytical Processing) systems play a vital role of analytics in many industries today. By aggregating the individual records of a data set, they provide an non-rational multi-dimensional view on the large volumes of data stored and are used for the purposes of analysis. Recently, the increasing availability of machines with large amounts of main memory and improving processor speeds have led to a surge in the popularity of in-memory OLAP systems like **S**calable **i**n-**me**mory **a**ggregatio**n**(**SIMEAN**) by R. J. Kopaczyk et al.[3], which can process multi-dimensional queries faster than their on-disk counterparts. However, while hardware capacities improve,

the amount of data to analyse continues to increase. We can imagine that technological inventions in the area of hardware resources may not be able to keep up with this growth and eventually could reach a halt. Rather than buying the newest cutting-edge machines every time, a better answer to the problem of data volume growth can be to enable a solution to scale out. This means that computation can happen by using a cluster of relatively cheap commodity hardware. Additional hardware machines can then be connected to handle even larger amounts of data.

The Problem: Continuously Growing Data Volume:

While storage capacity and access speeds for various medias (not only main memory) are growing dramatically, and processing speeds of processors have continued to improve, the amount of data collected, stored and analysed over a period of time has not remained at a constant level, either. Will the advantages gained by recent improvements of hardware performance soon be dissipated by the growth in data volume?

The Solution: Distributed Computing?

A naive solution to the problem of continuous data volume growth would be to just buy a better and more expensive machine if storage space runs out and/or processing time becomes inadequate. After all, one may argue, computing hardware gets better every year. However, there are good reasons why this solution may not prove to be viable in the long term:

1. Who guarantees that technological innovation will keep up with the data

growth rate? We can, after all, imagine that Moore's Law will not continue to hold forever. Also, this does not help if the rate of data volume growth exceeds the growth in matching hardware capabilities.

2. Buying highly specialized cutting-edge hardware machine is bound to become expensive, as the newest products in the market are usually sold at higher prices.

There is a cheaper alternative to this. We can buy several low-cost commodity machines, connect them together and make them work to achieve both higher storage capacity and better processing speed at a low cost i.e. distributed system. This also solves the first problem: although there is certain coordination overhead between nodes in a distributed system, we can continue to scale our systems independently of the speed of innovation. J. Bernardino, et al [4] proposed distributed system to improve query performance in OLAP which works on parallelizing queries. Golfarelli M. [5] proposed technology such as BPM (business process management) over the data-warehouse. C. Burnay et al. [6] proposed a framework for designing a system for business analysis by using the OLAP concept. It represents KPI's as facts and aggregation results as measures and schema for hierarchically organizing KPI's.

II. OLAP CONCEPTS

OLAP systems helps in planning, problem solving and decision making. OLAP deals with large amount of historical data. OLAP queries need to access large amount of data and need to perform huge number of aggregation. Following are some concepts used in OLAP systems.

A. Cube

For analysing data we use cube in online analytical processing (OLAP) as shown in Fig.1 and Fig.2. OLAP cubes are more famous in analytics for its feature of aligning data in multiple dimensions. These cubes are used to arrange the collected data for easy analysis purpose. This cube can be of type ROLAP, MOLAP or HOLAP. These cube categories are formed on the basis of storage of aggregation results. MOLAP stores source data and
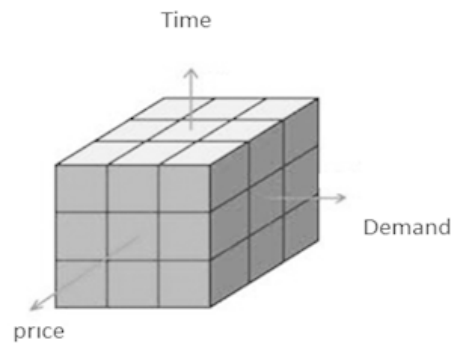
Fig.1 OLAP cube

aggregation results into multidimensional structure, ROLAP stores aggregation results into relational data store, whereas HOLAP is hybrid of ROLAP and MOLAP. We used ROLAP cubes to analyse the data. Each ROLAP cube has set of dimensions, measures, attributes and hierarchies as shown in Fig. 3. Dimensions represent the various fields of data to be analysed. Each dimension has its attributes. These dimensions can be of high cardinality. Dimensions can also be time dimensions whose attribute value is a time value.
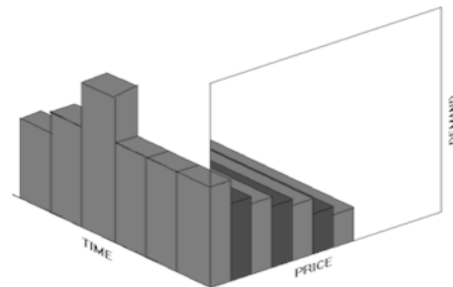
Fig. 2 OLAP cube with multiple dimensions

B. Hierarchy

In ROLAP cube, hierarchy is subset of dimensions arranged in the hierarchical manner for which aggregation values are to be computed. Each hierarchy represents the analysis perspective of a cube. To analyse cube for a hierarchy of dimensions it need to compute aggregation operation at every dimension level called measure or metric. A single hierarchy may have one or more measures. Attributes are values of dimension. Cube can contain multiple hierarchies. Level represents the level of dimension in the hierarchy. These cubes can be represented in the XML format. XML file can contain more than one cube representations. Each hierarchy

has its own set of dimensions as well as measurements.
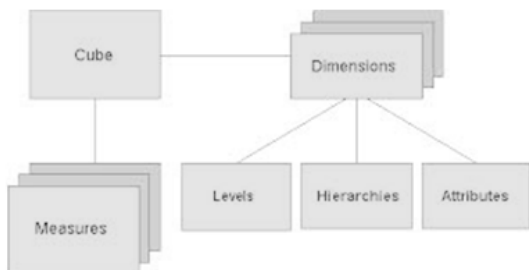
Fig.3 Architecture of a cube with showing its facets

```
<Cube>
      <Hierarchy>
            <Dimensions/>
            <Measurements/>
       </Hierarchy>
      <Hierarchy>
            <Dimensions/>
            <Time Dimensions/>
            <Measurements/>
      </Hierarchy>
</Cube>
```

C. Metrics

Metrics are the quantifiable measures that are used to track and assess the status of a specific business process. Every area of business has specific metrics. These metrics are nothing but the aggregation computations performed on the KPI's at every dimension level in a hierarchy. Metric can be any mathematical measurement such as Sum, Average, MAX-MIN, Standard Deviation etc. These metric functions depend on the analysis to be done.

Fig 4 Tree representation of hierarchy with metric node
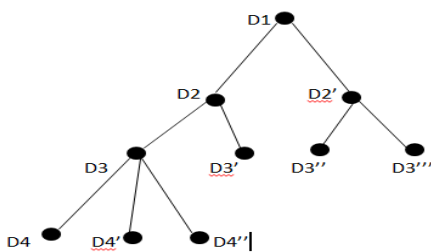
D. Metric Node

As shown in Fig. 4, it represents the tree structure for a hierarchy. D1, D2, D3, D4 are the levels of dimension in the hierarchy. These dimensions are arranged in hierarchical manner. D2', D3', D3'', D3''', D4' and D4'' are different values of attributes for the respective dimension levels. Thus branching in the given tree depends on the cardinality value of each dimension level. Node in the tree is identified by its hierarchical key formed by its position in the tree. e.g. for D4' node $D1\_D2\_D3D4$ will be the key. Each node contains the values computed for the aggregation metrics for its dimension level therefore these nodes are called metric nodes. Higher level node represents the aggregation of metric nodes below that level. Thus in a hierarchy every metric node is a unique entity and it is the lowest granularity of output entity.

III.   **PARALALLIZATION APPROACHES**

A. Based on input data partitioning

In this approach of parallelization, the input data is divided into non-overlapping parts and partial results are computed for each part. The process of aggregation is, in most cases, simple to parallelize. For performing aggregations in parallel we have to split the input into several non-overlapping parts and process them independently. There may be special design requirements when parallelizing the aggregation and this mainly dependent on the aggregation function used which we want to run in parallel for parallelizing it. Some of the aggregation functions such as sum, minimum or maximum of measures etc. are trivial. All of these functions are binary operator functions and satisfy the associativity property. In other words, the order in which the operations are performed does not matter. There are other aggregation operations which are not easy to parallelize but some of these operations are derived operations which use basic aggregation operations as their basic components. For example, average is the derived aggregation operation of sum and count which again use operator which are associative in nature that's why parallelizing average aggregation operation is not a tedious job. Likewise other operations can be parallelized. This parallelization strategy is solely based on input data partitioning but there are some holistic aggregation operations like TOP-K which are non-trivial and not easy to parallelize by input

data partitioning. Due to this limitation this parallelization strategy is not useful.

B. Based on input data partitioning

This approach of parallelization is to parallelize the computation based on the output partitioning. In this approach parallelization is done by computing each non overlapping output entity separately.

IV. PROPOSED WORK

Fig. 5 shows the architecture diagram of proposed system. In the proposed work we used second approach to parallelize analysis of continuously streaming multidimensional time series data according to the dimensionality of OLAP cube [2], to compute measures required for analysis of cubes due to the presence of holistic measures. In this method we parallelized analysis of cube at three places.

At first place we distributed the set of hierarchies to each node in the cluster. Each node will read the configuration of hierarchies to be computed. This distribution is a named distribution i.e. aggregation for any hierarchy can be computed by any computing node if it is enabled for computation on it. In this use case some of hierarchies are highly computation intensive while some are not. So to avoid skew problem we made a unit of two hierarchies for distribution in which one hierarchy is computation intensive and other is not. Hierarchies are distributed to nodes according to these units.
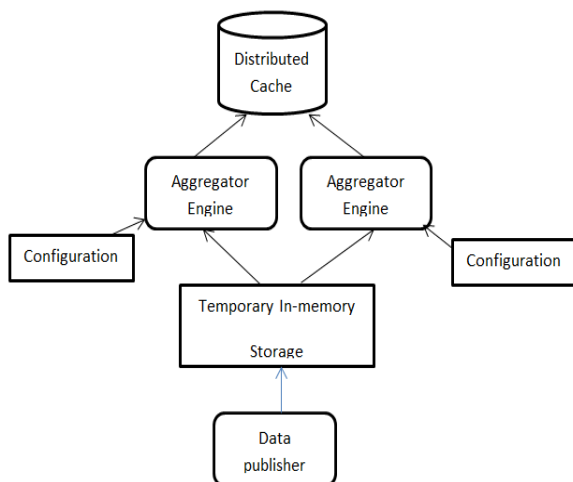
Fig. 5 Architecture of proposed system

In this method, we created a data publisher to send the continuously streaming KPI's called Facts represented in the form of multidimensional time series data. The data received from the publisher is temporarily put into the in-memory storage. These in-memory KPI's are forwarded to each subscribing nodes in the cluster by listening to the put operation preformed in in-memory storage.

In proposed work we have multiple cubes to analyse with one or more hierarchies in each. Streaming multidimensional KPI's for each cube are identified by matching its set of dimension. At second and third place we parallelized analysis of cubes by computing aggregation operation at each dimension in a hierarchy for this purpose we used actors concurrency model.

1. Concurrent Actors

Today the use of actor based concurrent models is on the peak. Typesafe's AKKA[1] is an open source framework used for real time transaction processing. It is a highly scalable and highly concurrent actor based model. AKKA actors are lightweight entities with
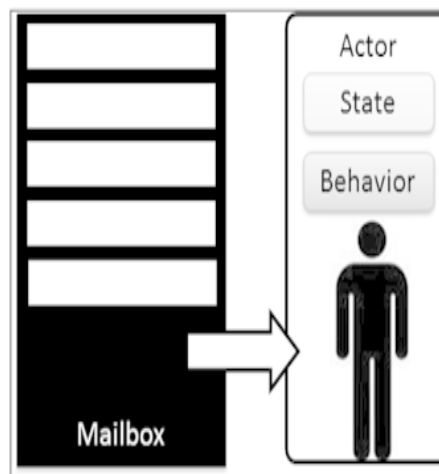
Fig. 6 Architecture of actors in actor based model

asynchronous and event driven processing. Each AKKA actor has its mailbox which can be bounded as well as unbounded. Actors can be created for performing highly concurrent tasks. These actors can be state-full as well as stateless. Actors receive tasks in the order as message in the mailbox. These received messages are identified by using pattern matching. Behaviour of AKKA actors can be defined according to the received message. These actors can be identified in the cluster by using its name as unique id. In-order to achieve maximum concurrency in an application we

have to create a thread for its lowest granularity of tasks. Creating large number of threads is not feasible in case of the highly concurrent tasks due to the overhead of maintaining concurrency while using large number of threads. So, in this method at second place of parallelization we created multiple concurrent actors to create batch of tasks and grouped by using the key. This batch of tasks identified by key is distributed to actor identified by same key as name because of this specific type of task is always distributed to specific actor which will guarantee the in order processing of message according to their arrival time.

At third place of parallelization we used AKKA actors to compute and update aggregations for each metric node in the hierarchy tree. AKKA actors are created for lowest granularity i.e. metric node. Actors created executes concurrently to achieve maximum thread utilization. Actor will compute the aggregations results using previous value present in persistence used and KPI values in the multidimensional streaming data. These updated aggregation results of each metric node are stored in the in-memory storage to reduce disk-access delays.

V. EXPERIMENTAL SETUP AND RESULTS

For Experimental setup we used two machines with Intel i7, 2 core and 8GB RAM as two processing nodes. We measured the rate of streaming KPI's processed per second at an average use of 30% of CPU. We used the "thread-pool-dispatcher" as dispatcher service in AKKA actors. Graph in Fig. 7 shows the variation of processing rate with the distribution of number of hierarchies on each node.

VI. CONCLUSION

The applications and profits earned from online analytical processing (OLAP) clearly shows that it is one of the emerging revolutionary technology trend that can be used extensively in managing and analyzing data to get vital information and knowledge. All businesses, big or small, The instant access to information and the apparent
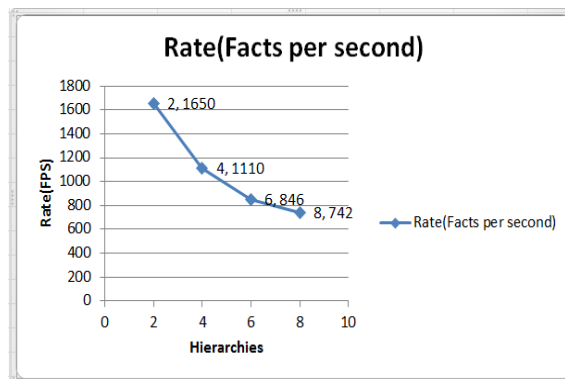
Fig. 7 Results obtained by distributing hierarchies

knowledge gained from the analyzed information is priceless considered against the cost involved in establishing such a setup. Increasing speed of OLAP by distributing its aggregation computation using commodity hardware will increase the cost effectiveness of such applications. Due to use of streaming KPI's it will be online, real-time

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A SURVEY ON IDSS IN MANETS

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Abstract— **With the changing age of technology we are observing magnificent changes in the way of communication. We are speedily moving from the wired networks to the wireless networks, in the last decade there has been drastic increase in the use of wireless networks due to the great development of mobile technology and its efficiency to connect the world significantly. Mobile Adhoc Networks (MANETs) are playing crucial role in this transformation. They being infrastructure less networks are really useful in the mission critical applications like military and the areas where the natural calamities have occurred. In MANETS as each node can behave both as receiver and transmitter the formation of the network becomes very easy. regardless Of all the advantages MANETs are pretty vulnerable as per the security attacks are concerned ,as it is having free medium intruders can easily enter the medium and attack the system. Intrusion Detection Systems(IDS) are specifically designed to stop such kind of attacks on the system.these systems(IDS) find out the vulnerable nodes and prevent them from making the great damage to the systems Watchdog ,TWOACK, AACK,EAACK are some of the IDS used now a days. Further the use of hybrid cryptography has added extra security to it.**
Keywords- MANETs, Intrusion Detection System, EAACK

1. INTRODUCTION

MANETs are the collection of mobile nodes equipped with both transmitter and receiver and communicating over a bidirectional wireless link directly or indirectly. Depending on the communication range MANETs are divided into two types. If all the nodes in the network are in communication range and can communicate directly then they form Single-hop netwok [1]. While if for sending messages from one node to another node they have to go through the another nodes they form multi-hop network.

All the nodes in these networks rely on each other for transmission of data in the network. Introduction of some misbehaving nodes can bring the throughput of the network by substantial amount. Though MANETs are having self organized and self maintained network formed without any infrastructure it is having a great threat about the security measures [3]. Intrusion detection systems play vital role in removal of security threats. IDS monitors the behavior of different nodes and find out whether there is some node which is performing some malicious actions and causing problems for the networks. Some IDS work on basis of just monitoring the nodes while some work on the basis of responses like acknowledgements. As there is no physical protection to the network the intervention of intruders is quite easy in these types of networks because most protocols used in the MANETs assume every node in the network behaves cooperatively and not malicious. The sad thing about security is that many organizations in the world invest less in security issues than they are investing on the other common stuff as it is not providing any direct revenue due to this the security is too poor which further boosts the intruders.

2. IDS in MANETs

As discussed above due to the assumptions of routing protocols in MANETs that all the nodes behave co-operatively, MANETs become very easy to attack just by compromising one or two nodes. This is the reason IDS should be added to improve the level of security in the MANETs by removing the compromised nodes in the network. Some of them like Watchdog, AACK,TWOACK will be discussed in this paper.

2.1 Watchdog:

Watchdog is a scheme that is designed in way that it will improve the throughput of a network though there are malicious nodes in the network which are trying to bring down the performance [4]. Watchdog consist of two parts Watchdog and pathrater. Watchdog works as a IDS for MANETs. It continuously listens to the nodes in the network
and keeps eye on the malicious activities of the next nodes in the network. If it find out that the next node which is overheard is not transferring the packet to the subsequent ones then it increases the failure counter for that node. There is a predefined threshold defined for failure counter. If the failure counter crosses the threshold value tht node is declared as a malicious node by Watchdog. In this case the pathrater comes into act ,with the help of routing protocols it finds the new path for the transmission of packets so that the malicious node is avoided.

Studies have shown that Watchdog scheme is an efficient one[9][10][11]. What makes it more special is that it detcts the malicious nodes rather than the links. Watchdog has been appreciated and taken as a reference by many other IDS. The new system were developed either taking it as a base or improving the problems with it.

Though it is taken as a reference it is having certain problems [1] to figure out the malicious nodes in the following conditions . 1) Ambiguous collisions; 2) receiver collisions; 3) limited transmission power; 4) false misbehavior report; 5) Collusion; and 6) partial dropping.

2.2 TWOACK:

Many different researchers came out with their ideas to solve the problems with the Watchdog.

TWOACK is one of the approach which was proposed by Liu et al[]. The difference between this method and others is that it is neither enhancement nor a scheme having its base as a watchdog. Watchdog finds out the malicious node but this system is more concerned about the links. It is an acknowledgement based scheme which works with the three consecutive nodes at a time. As soon as node receives a packet it has to send back acknowledgement to the node two hops down the route from it. TWOACK works with the dynamic source routing protocol.
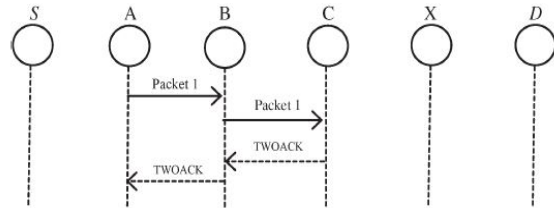
Fig1:TWOACK scheme

The figure shows how the TWOACK system works packet 1 is transmitted from A to B, B further pass it down to C. As soon as C receives the packet and it being two hop away from the source it sends back TWOACK packet down the line to A. The arrival of packet at A is indication that the packet has been transferred upto C successfully. If A doesnt get TWOACK packet in predefined time it reports both B and C as malicious nodes.

The TWOACK scheme solves the receiver collision and limited transmission power problems of Watchdog, but it creates excessive amount of acknowledgements which creates excessive overhead on network. It can create a lot of energy problems.

2.3 AACK:

This method which is based on the TWOACK method was proposed by Sheltami *et al* [4].This method is combination of two schemes TACK which is similar to TWOACK and ACK which is an end to end acknowledgement scheme. It substantially reduces the network traffic and perform as good as or sometimes better than the TWOACK.
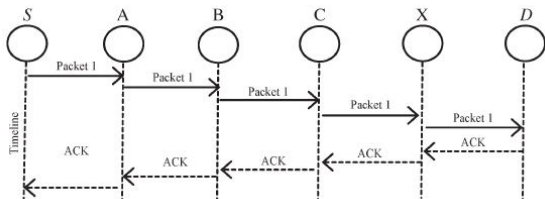
Fig.2 ACK scheme.

ACK scheme works as per shown in above figure 2. The source S has sent a packet for node D. The intermediate nodes just forward the packet to the next node. As soon as node D receives the packet it has to send back the packet to the node S in the reverse order of the same path. If S receives the packet in a predefined time period then transmission is successful otherwise S will move to the TACK mode. Using this hybrid technique we lower the network traffic by a great margin. Though this is the thing main problem with both TWOACK and AACK is that they suffer from the problem with the false misbehavior report and forced acknowledgements.

3. DIGITAL SIGNATURES

As we are using open medium in the MANETs security is a major concern for this. It is necessary to check whether the packets we have got are authentic or not. It will be secure if we communicate by using encrypted messages by using cryptographic methods. For integrity, authentication and nonrepudiation we use Digital Signatures. We use public key cryptography and hashing for creating Digital Signatures.

4. EAACK

EAACK is IDS for MANETs which is designed to solve three out of six problems in the Watchdog receiver collision, limited transmission power and false misbehavior report.
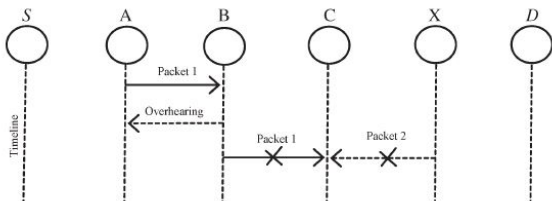
Fig3.Receiver collision
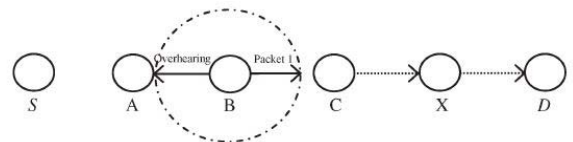
Fig.4. Limited Transmission Power
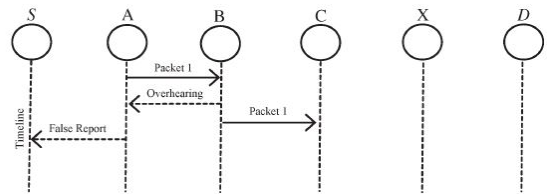
Fig.5 False Misbehavior report

The above three diagrams show the three problem with the watchdog

4.1 Receiver collision:
fig.3 shows what exactly the receiver collision problem is. Node A sends the packet to node B. It further overhears whether B has forwarded the packet to C. At the same time node X is also sending packet to C. In such a case A overheard that packet has been successfully forwarded by B, but it fails to detect that node C has failed to receive the packet due to collision at C.

4.2 Limited Transmission Power:
In this case a node behaves selfishly; it limits its transmission power so that it can be overheard by only certain nodes. As shown in fig. 4 node B limits its transmission power so it can be overheard by A but not by the node C.

4.3False Misbehavior Report:
In false misbehavior report node A has sent packet 1 to B which B has forwarded successfully to C still A has reported B as misbehaving node as shown in fig. 5.

TWOACK and AACK can solve the first two of these three problems but fail for the third one. EAACK solves the three problems more promisingly.
EAACK is consisting of 3 major phases ACK, Secure ACK(S-ACK) and misbehavior report authentication (MRA).The packets are distinguished using two bits packet header included in EAACK.
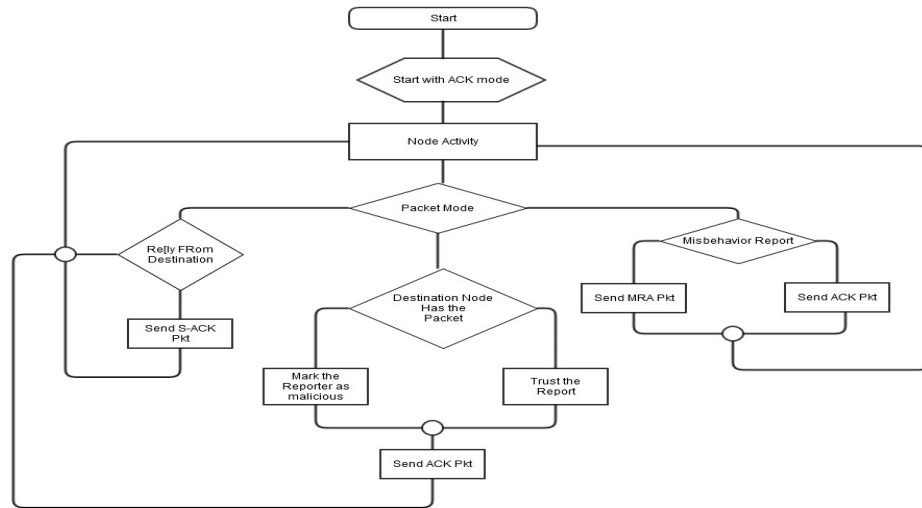
Fig.6 EAACK scheme

Fig.6 EAACK scheme
Above figure illustrates the working of the EAACK scheme. It goes through the three different phases before reporting a node as a malicious.

4.4 ACK:
ACK in general is an end to end acknowledgement scheme, here it works as a part of hybrid scheme to minimize the network overhead when everything is working fine. In this case the source sends a packet to destination if all the intermediate nodes cooperate then the packet will be forwarded to the destination. Destination has to send back the acknowledgement to the source in a predefined time so it is assumed to be successful. Otherwise the source has to switch to the S-ACK mode.

4.5 S-ACK:
After the node fails to receive an acknowledgement it switches to the A-ACK mode which is improved version of TWOACK scheme .The group of three consecutive nodes is taken in consideration to find out misbehaving nodes.
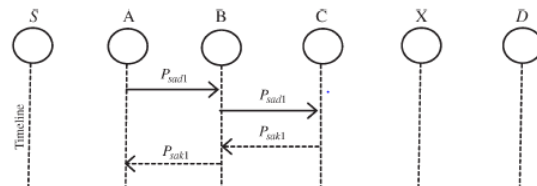
Node A has sent the S-ACK data sad1 to B which it has transferred to C as the node C is two hops away from the source it has to send back S-ACK acknowledgement packet back to the A on the same path. If acknowledgement is not sent back to A, it will send misbehavior report to the source S.
At this time source will move to MRA mode.

4.6 MRA :
This is vital step in the EAACK scheme to detect false misbehavior of the nodes. Some nodes may send false misbehavior report which will be indicating the nodes as a malicious nodes falsely.
        In this mode the source node checks its local database to check whether there is another path for that destination node. If there is no such path existing then it will start DSR routing request. By doing this we will reach the destination by another path. After receiving the packet receiver will check its l
destination the misbehavior report is wrong otherwise it has to be trusted.

4.7 Digital Signature:
All the three parts are acknowledgement based schemes. They all believe on Acknowledgements to detect the malicious

nodes in the network so it is so much important to check the authenticity of the packets. Digital signatures provide the required authentication in this scheme. DSA and RSA are used for this.

5. PERFORMANCE METRICS
The performance of the different IDS can be measured on the basis of the following metrics.

5.1 Packet delivery ratio (PDR):
PDR defines the ratio of the number of packets received by the destination node to the number of packets sent by the source node

5.2 Routing overhead (RO):
RO defines the ratio of the amount of routing-related transmissions [Route REQuest(RREQ), Route REPly (RREP), Route ERRor (RERR), ACK, S-ACK, and MRA].
We can check performance of the systems in different scenarios like packet dropping and false misbehavior.

6. CONCLUSION
Security has become a great concern in MANETs
And we are coming across different types of IDS day by day. In the studies we found that WATCHDOG has been reference for most of these systems. It has been surrounded by lot of problems. TWOACK and AACK solve some of the problems but suffer from some problems like network overhead and false misbehavior report. EAACK has evolved as one of the best IDS which outperforms the other schemes substantially.
EAACK further adds the security to the communication and doing so helps to improve the faith in the users to use the network. The hybrid technologies are evolving as a reat source for the security.

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EFFICIENT SOLVER FOR LINEAR ALGEBRAIC EQUATIONS ON PARALLEL ARCHITECTURE USING MPI

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Abstract
Most of the problems in engineering science can be modelled using differential equations. However quite often, the differential equations are not amenable to direct analytical solutions because of complex geometries and boundary conditions. Thus recourse is taken to approximate numerical solution techniques. Depending on the discretization of the domain, the numerical model of the problem at hand could become very large – sometimes running into thousands/lakhs of degrees of freedom. Solution of such a large set of equations is a daunting task computationally and hence efforts are directed towards development of efficient strategies and use of High Performance Computing (HPC). The present work aims to implement an efficient solver for system of linear equations with sparse, symmetric and positive-definite matrix of coefficients using the most prominent Conjugate Gradient iterative method and study the performance improvement obtained in parallel computing framework using MPI and GPU enabled CUDA technologies considering a suitable example problem.
Index Terms: **Message Passing Interface (MPI), Compute Unified Device Architecture(CUDA), Finite Element Method (FEM), Conjugate Gradient (CG).**

I. Introduction

In the past few years, The Message Passing Interface(MPI) and GPU(Graphics Processing Unit) enabled CUDA(Compute Unified Device Architecture) is being widely used to develop parallel programs on computing systems such as clusters. Recent advances in high performance computing resources, programming environments for parallel architecture are well suited to perform massively parallel computation on the large set of equations. In this paper, we focus on solving large set of linear algebraic equations of the form

$$Ax=B \qquad (1)$$

Where the known n-by-n matrix 'A' is sparse, symmetric (i.e. A^T=A), positive definite (i.e.x^TAx > 0 for all non-zero vectors $x \in R^n$), and real, and 'B' is known right hand side vector.

The equation arises in various fields of engineering science such as complex structural analysis problems in aerospace, civil and mechanical engineering disciplines; complex fluid flows for example in aerospace, ocean modeling for tsunami applications, blood flow etc. To render them suitable for computer based solution, approximate numerical techniques are often deployed. Efficient solution of such a large set of algebraic equation enables us to build models that are as close to reality as possible, thus enhancing

our understanding of scientific problems. Computer based modeling and simulation is recognized as the third pillar/paradigm of scientific development. These linear algebraic equations can be solved by direct method (Gauss Elimination, LU decomposition etc.) or by iterative method (Steepest Descent, Conjugate Gradient)[1].The Non-stationary iterative method (Conjugate Gradient, preconditioned Conjugate Gradient) are more accurate than Stationary methods (Jacobi, Gauss-Seidel)[2]. These methods are widely used to solve many important settings such as finite differences, finite element method [3] for solving partial differential equations and structural and circuit analysis.

The outline of the paper is as follows. Paper includes a summary of prior works which includes iterative methods (CG) to solve system of linear equations, proposed work and finally conclusion.

II. Literature Survey

2.1 Conjugate Gradient Method:

The Conjugate Gradient is the most widely used iterative method to solve system of linear equations of the form

$$Ax=B$$

Where, 'A' is symmetric and positive definite matrix, 'x' is unknown vector and 'B' is the known vector. The iterative method like CG are suited for use with sparse matrix and if matrix is dense then direct method using substitution are efficient then iterative methods. The CG will take at most 'n' iterations to reach to the exact solution. The algorithm for CG is shown in fig.1.

let, initially assume unknown vector $x_0 = 0$, where each direction vector 'p_k' gives new approximate 'x_{k+1}' and also error 'r_k'. In each step, using this error, the previous direction and the property that any two directions are conjugate to each other we find a new direction. We repeat this process till the error 'r_k' is sufficiently small.

Step 1: Initialization
$$r_0 = b - Ax_0$$
$$p_0 = r_0$$
$$k = 0$$

Step 2: Step size (directional coefficient)
$$\alpha_k = \frac{r_k^T r_k}{p_k^T A p_k}$$

Step 3: New Approximation to x
$$x_{k+1} = x_k + \alpha_k p_k$$

Step 4: Calculate error
$$r_{k+1} = r_k - \alpha_k A p_k$$
If r_{k+1} is sufficiently small then exit loop end if

Step 5: Direction update coefficient
$$\beta_k = \frac{r_{k+1}^T r_{k+1}}{r_k^T r_k}$$

Step 6: Calculate new direction
$$p_{k+1} = r_{k+1} + \beta_k p_k$$
$$k = k + 1$$

End Repeat

Result is x_{k+1}
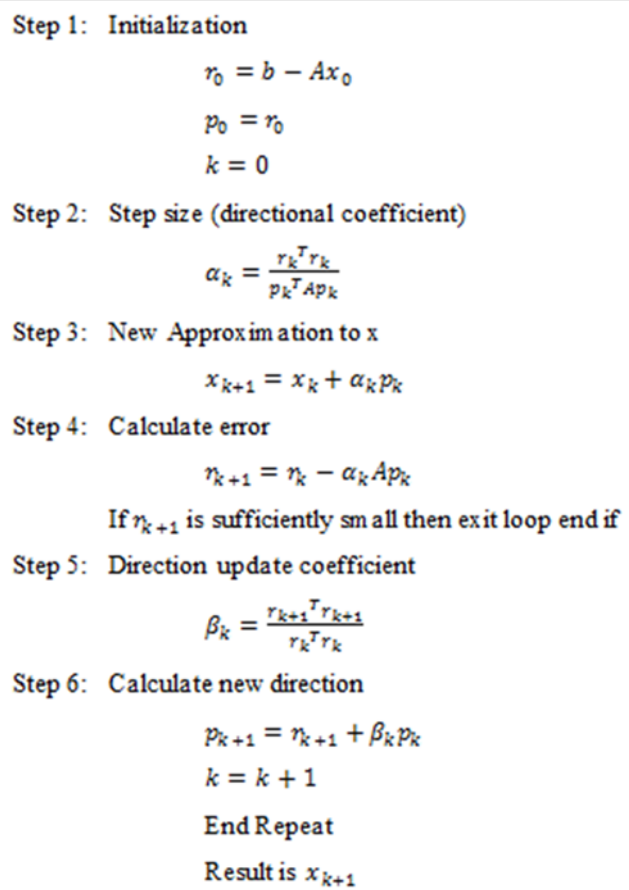
Fig. 1 Conjugate Gradient Algorithm.

The CG method requires one SpMV and two inner products. The most time-consuming part of this algorithm is multiplication of sparse matrix 'A' and dense vector 'p', hence efforts are directed towards parallel computation and also it is more efficient to store only the non-zero elements of a sparse matrix. There is a number of common storage formats used for sparse matrices discussed in [4].

III. Message Passing Interface

MPI[6] is language independent communication protocol used to program on parallel computers to scale the performance of the application. Message passing is an activity where the processors coordinate their activities by explicitly sending and receiving messages by the functions MPI_Send and MPI_Recv. It is the most common method of programming distributed-memory MIMD system. MPI is considered today's standard in message passing library.

IV.   Sparse Matrix Storage Format

The matrix that arises from the discretization of the differential equation has a large dimension, usually more than thousands by thousands in size and it is also sparse, and so a good sparse matrix format doesn't only reduce the space requirement, but also enables faster sparse matrix operations. Moreover, since most of the simulation time is spent on solving sparse linear system equations, choosing a good sparse matrix format is essential to facilitate faster sparse matrix solvers.

$$\begin{bmatrix} 12 & -6 & 0 & 0 & 0 & 0 \\ -6 & 6 & -6 & 0 & 0 & 0 \\ 0 & -6 & 6 & -6 & 0 & 0 \\ 0 & 0 & -6 & 6 & -6 & 0 \\ 0 & 0 & 0 & -6 & 6 & -6 \\ 0 & 0 & 0 & 0 & -6 & 6 \end{bmatrix}$$

Fig. 2 Sparse Matrix.

Compressed Sparse Row (CSR) is popular and the most general purpose storage format. This can be used for storing matrices with arbitrary sparsity patterns as it makes no assumptions about the structure of the nonzero elements. Like COO, this format also stores only nonzero elements. These elements are stored using three vectors: 'val', 'col' and 'row_ptr'. The 'val' and 'col' vectors are same as for the COO format. For an 'M*N' sparse matrix, the 'row_ptr' vector has length of 'M+1' and stores indexes where each row of the matrix starts in the 'val' vector. The last entry of 'row_ptr' corresponds to the number of nonzero elements in the matrix. There are some advantages of using CSR over COO. The CSR format takes less storage compared to COO due to the compression of the row indices explained in above Figure. Also, with the 'row_ptr' vector we can easily compute the number of nonzero elements in the ith row as 'row_ptr'(i+1) − 'row_ptr'(i).

In parallel algorithms, 'row_ptr' values allow fast row slicing operations and fast access to matrix elements using pointer in direction. This

is a most commonly used sparse matrix storage scheme. This is explained below:

Index	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Val	12	-6	-6	6	-6	-6	6	-6	-6	6	-6	-6	6	-6	-6	6
Col	1	2	1	2	3	2	3	4	3	4	5	4	5	6	5	6

Row_ptr	1	3	6	9	12	15	17

V.   Proposed Work

The present work aims to implement an efficient solver for linear algebraic equations and study the performance improvement obtained in a parallel computing framework using a suitable example of 1D Bar problem using FEM (Finite Element Method).

Solving FEM problem divided into following steps
1. Divide problem into number of finite elements.
2. Generate local stiffness matrix.
3. Assemble to form the linear systems of equations of the   form Ku=f
4. Solve this linear system of equations by CG method
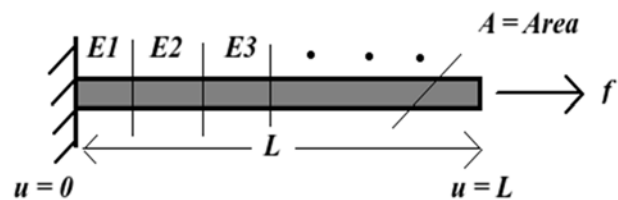
Fig. 3 1D Bar Problem

Solutions to static linear structural mechanics problems reduce to solving a linear system of equations of the type:

$$[K]\{U\} = \{F\}$$

Where 'K' is global stiffness matrix, 'U' is a global displacement vector, and 'F' is the global force vector. One end of bar is fixed and force (f) is applied at other end of bar. Bar is divided into 'n' number of finite elements area of cross sections area (A) at each element. Hence the matrix 'K' which will be generated will be of size n.Equation 'Ku=f' is then solved by CG/PCG to

calculate displacement vector 'u'.

The memory requirements and the computational time required to solve such equations increases as the number of equations increases. To deal with such large numerical problems in the Finite Element Analysis, parallel computing on high performance computer is gradually becoming a main stream tool. Many parallel algorithms and programs for finite element computation have been developed on parallel computers, utilizing vast numbers of CPUs or GPU cores to achieve high speed up and scalability.

VI. Parallel Implementation of CG Algorithm

Since CG, is an iterative method, the result of next step is depend upon its previous step, hence it is hard to simultaneously compute intermediate steps, so we focused on distributing the data across processor and ask them to involve in the computation of its local part. As CG algorithm involves two dot products and one matrix vector multiplication per iteration and it can be easily parallelized by using following MPI communication operations:

Step1: Read the Matrix stored in CSR format and Right hand side Vector from the file and divide it across processors using MPI_Bcast and MPI_Scatterv.

Step 2: All processors will compute the dot product locally and do a sum reduction using MPI_Allreduce.

Step 3: In Matrix Vector multiplication all processors requires complete vector and this vector is getting updated after each iterations. So do multiplication in parallel using MPI_Allgatherv, to gather all the local parts of the vector into a single vector and then do the multiplication.

Also, one can used MPI_Send and MPI_Recv to gather vector but MPI_Allgatherv is known to be an efficient way to communicate between processes.[6]

But, as we are dealing with only 1D bar problem which generates tridiagonal matrix, in this case MPI_Allgatherv would not be efficient because every processor requires only one or two elements of vector P to carry out matrix vector multiplication, so we used MPI_Isend and MPI_Irecv to avoid communication overhead.

VII. Results

As the most time consuming part of conjugate gradient method is SpMV, so to optimize Sparse matrix vector multiplication we have used CSR sparse matrix storage format which allow us to perform operations only on the nonzero elements present in the matrix. Figure (4) shows the comparison of sequential and parallel implementation using MPI of Conjugate Gradient method for different sizes of tridiagonal matrix.
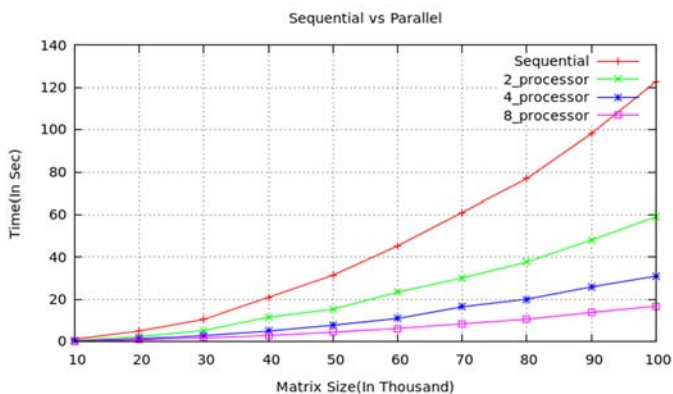

Fig. 4 Sequential vs Parallel

Figure(5) shows the scalability of parallel code executed on 2 node cluster which has total 4 cpu's and 8 cores's/cpu with matrix size N=504000 having non zero elements NNZ = 1511997 and the speedup of parallel conjugate gradient method is shown in Figure(6).
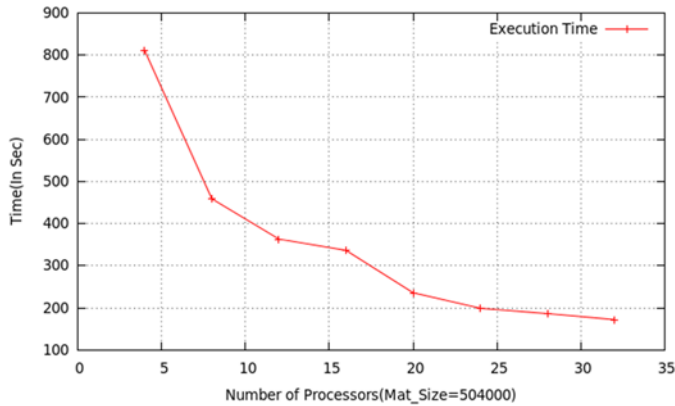
Fig. 5 Scalability of Parallel CG
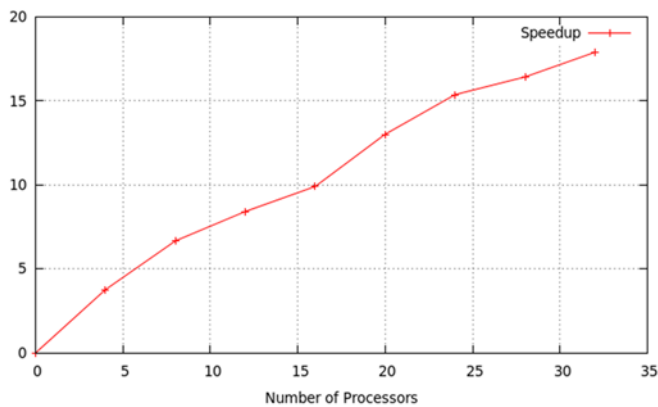
Fig. 6 Speedup

VIII. Conclusions

In this project we have implemented a parallel version of the Conjugate Gradient method using Message Passing Interface and have tested it for various sizes of tridiagonal matrix. Although we could have used various libraries such as SCALAPACK, PETSC for the implementation of CG, but instead we choose to implement it by our self so that we can be familiar with the issues while developing parallel CG. So, according to us there may be some communication overhead either in MPI_Allgatherv or MPI_Isend and MPI_Irecv whatever is used according to input matrix. So efficient communication is must while dealing with such huge sizes of matrices while solving linear algebraic equations.

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SELECTED RESEARCH PROBLEMS IN THEORETICAL COMPUTER SCIENCE

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Abstract— Working in the core areas of computer science has always been difficult, especially for beginners. Difficulty arises in finding a research problem and to understand the research process, as one should have complete understanding of the field in order to pursue research. In this paper, we present some selected research problems in theoretical computer science those having much practical use. This paper is to generate the research interest in beginners to work in this field. After going through the paper readers will be able to bank their research objective, ideas to pursue, and important articles for creating their basic foundations. We also present examples for better understanding, and directions to position the research work.
Index Terms—Theoretical Computer Science, Formal Languages, Lazy Learning, N-gram, Machine Translation.

I. INTRODUCTION

Research in theoretical computer science mainly deals with the study of mathematical concepts and concerns in obtaining computational models for the formulation of problems. It also derives its motivation from practical aspects and computation. Research results require mathematical proof and rigorous analysis in order to support its validity and soundness. Accuracy of research results requires to go for implementation of abstract model with benchmark data sets in order to see how results compare with others. After the invention of Turing machine algorithms are considered as a set of computational steps. Thus, the research process in this area can be viewed as to give an algorithmic model of computation for the problem under study; then we need to show it correctness, analysis and finally we should go for profiling works for the confirmation of theoretical analysis and positioning the work.

Theoretical computer science is a broad field within general computer science. Research areas like algorithms, data structures, language theory, automata theory, parallel computation, Computational biology, machine learning, algorithmic learning theory, randomization, distributed computation, very large scale integration, computation complexity theory, etc. are regarded to fall in theoretical computer science field. The problems generally in this field are seemed to be computationally hard but interesting. Formulation of such problems requires having sound knowledge in the area.

In this paper, we discuss some notable problems that can be considered as a line of work. This will be useful for beginners those wish to peruse PhD (or research) and are in search of the problems to take as a research project.

II. LEARNING OF FORMAL LANGUAGES

Learning of formal languages, often called grammatical inference, is an active research area in machine learning and computational learning theory. In machine learning machine

seems to be learn by experience. The problem of learning a correct grammar for the unknown language from finite examples of the language is called grammatical inference. In particular, the problems of learning finite automata from positive and negative examples for the case of regular languages have been widely and well studied. Inductive learning of formal languages inherently contains computationally hard problems. For example, the problem of finding a deterministic finite automaton with a minimum number of states consistent with a given finite set of positive and negative examples is known as NP-hard [1]. The first convincing model for the case grammatical inference is introduced by Gold in 1967 [2]

The problem of inductively learning of context-free grammars from positive and negative examples is a more difficult learning problem than learning finite automata.

A grammar is a quadruple $G = (N, \Sigma, P, S)$, where N and Σ are the alphabets of non-terminals and terminals, respectively, such that $N \cap \Sigma = \emptyset$. P is a finite set of productions and $S \in N$ is a special non-terminal called the *start symbol*. A grammar G is called *context-free* if all production rules are of the form $A \rightarrow \alpha$, where $A \in N$ and $\alpha \in (N \cup \Sigma)^*$. In the production rule $A \rightarrow \alpha$, A is called as the left-hand side (LHS), and α is the right-hand side (RHS). A language L is a context-free language if there exists a context-free grammar (CFG) G such that $L = L(G)$.

If we are given plain text (i.e., positive examples of the language) and asked to determine the grammar consistent with the text then it is a difficult problem. As in the search space of grammars there are possibly infinite grammars. We need to exhaustively find all possible grammars and select that is consistent with input text. The difficulty arises from two specific aspects of the problem of learning context-free grammars from examples: first determining the grammatical structure (topology) of the unknown grammar, and second identifying the set of non-terminals in the grammar. The first problem is especially hard because the number of all possible grammatical structures for a given positive example becomes exponential in the size of positive examples. Thus, the hypothesis space of context-free grammars is very large—too

large in which to search for a correct context-free grammar consistent with the given examples. Sakakibara has shown that if information on the grammatical structure of the unknown context-free grammar is available for the learning algorithm, there exists an efficient algorithm for learning context-free grammars from only positive examples [3]. Otherwise there is no known polynomial time algorithm available for learning context-free grammars from plain text.

Grammatical Inference has its wide applications including Computational Biology. Natural language processing, learning programming languages, information extraction, pattern recognition, etc.

Difficulty of learning context-free grammars has given rise different methods including learning tree automata, artificial intelligence like approach using genetic algorithm, and using fuzzy similarity measure.

A. Learning Tree Automata

A **tree automaton** [3] is a type of state machine which deals with tree structures, rather than the strings (or words). On input structural examples, Sakakibara first constructed tree automata then using tree automata context-free grammar are constructed. Running time of this algorithm is polynomial in terms of the size of input skeletons (structural examples) [3].

B. Context-Free Grammars Learning Using Genetic Algorithm

A genetic algorithm is a guided random search technique used to find near optimum solution. Solution obtain using genetic algorithms may or may not be optimal. This technique seems better when search space is very large and brute force techniques fail to apply. Genetic algorithms use techniques inspired by evolutionary biology such as inheritance, mutation, selection, and crossover. Starting from the set of initial solution we go generation by generation in order to find the better solution.

Sakakibara and Kondo have used genetic algorithms (GAs) to search for a context-free grammar in Chomsky normal form, consistent with the given examples [4]. Experiments suggest that the knowledge of part of the structure (some parenthesis) may help and reduce the number of generations needed to

identify the correct grammar and thus contribute to improving the efficiency of the learning algorithm [5].

C. Context-Free Grammars Learning Using Fuzzy Similarity Measure

This is an alignment based learning. *Alignment based learning* (ABL) [6] is based on the alignment of sentences and substitutability. In the alignment phase the matched parts of sentences considered as possible constituents. Equal parts and unequal parts are used for generating context-free grammar production rules. Non-terminals are assigned as the left hand sides of the production rules with the unequal parts as the right hand sides shown by the following example:

[Ram] sees the [green] apple.
[Shyam] sees the [red] apple.

The created grammar rules are:

S → NT_A sees the NT_B apple,
NT_A → Ram,   NT_A → Shyam
NT_B → green,   NT_B → red

In particular, alignment profile is generated to obtain the consistent grammar [7]. However, learning context-free grammars from positive examples without using any heuristic information is still a challenging problem.

III. SEARCH IN HIGH DIMENSIONS

Nearest Neighbor (NN) search in high dimensional data is widely used method which has applications for image/information retrieval, medical imaging, DNA matching, pattern recognition, machine learning, data mining and many more. Search for high dimensional data/query in feature space is still a dimensionality curse [8] where probability of finding nearest neighbor decreases as number of dimension grows.

Accuracy of result is based on important factors like memory requirement, number of dimensions, clustering algorithm and many more. Further research is required in area of exact NN search methods which consider all features of data.

IV. CLASSIFICATION PROBLEM

Support vector machine (SVM) is applicable in many domains for classification. SVM classification is the main approach after that many researchers divert the path for accuracy and efficiency in SVM classification from using the analyzing features and kernel [9].

Many research done in SVM classification with selected features and kernel in different domain area; but some are related to feature, some are related to kernel and some are related to any particular application domain. Designing an efficient classifier is still an active research problem.

V. QUERY OPTIMIZATION TECHNIQUES

Query Optimization is very important function of Database Management System (DBMS). Query Optimizer translates user-submitted Query into different Query Evaluation Plans (QEPs). All plans are equivalent in terms of their final output but vary in their cost, i.e. the amount of time that they need to run. Query Optimizer explores different plans and attempts to determine most efficient plan for executing the query. The Process of creating, exploring and selecting an efficient plan is called Query Optimization. The Query Optimizer in standard DBMS picks a single Plan and executes Query with the selected plan. The chosen plan aims to minimize running time by carefully optimizing the use of secondary storage, memory, and CPU [10].

Now days Databases are growing exponentially with increasing complexity to manage wide variety of local and global Data, static and dynamic Queries, large datasets, large number of operators. More statistics, more metadata required to handle so many number of tables, relations, attributes. An optimizer is required to select an efficient plan among thousands of plans. Moreover, plans at optimization and execution time increase and hence computational cost increases as well as performance of an optimizer may not be optimum. Therefore obtaining an efficient optimizer is still a challenge.

Now scientists have gone to Adaptive query processing technique as it focuses on using runtime feedback to modify query processing in a way that provides better response time or more efficient CPU utilization [11]. Several Adaptive Query Processing Techniques have been developed to address the query processing issues

[12]. Adaptive Query Processing techniques still not capable of handling complete issues so other query processing techniques including obtaining information not stored in the catalog and providing it just-in-time to the optimizer [13], learning from past queries and mistakes [14], Clustering and using techniques from data stream systems can be combined together to reduce query processing problems [10]. Thus beginners may take this line of work in order to obtain an efficient query processing scheme.

VI. LAZY LEARNING APPROACHES

Lazy learning approach for classification also provides ample rooms for research. Classification is one of the important techniques of supervised learning, which is used to predict categorical class labels. It mainly classifies the data (constructs model) on the basis of data provided for training with class labels and uses it to classify new data. Many effective classification algorithms have been developed such as Decision tree, Naive Bayes, Neural networks and so on.

In general a classifier may generate large number of rules satisfying some quality constraints. However, during classification many of these generated rules may be useless and worst. Lazy (non-eager) learning classification overcomes this problem by focusing on the features that actually occur within the testing instances. Lazy learning classifier is to establish a classification of the rules for features that actually occur within the testing instances and to increase the chance of generating more rules that are useful for classifying the test instance. In literature, we can see different lazy learning approaches [15]. As a future research one can consider to work on improving computing efficiency of Lazy learning classifiers, for which the computation is performed on a demand driven basis.

VII. BIOLOGICAL COMPUTATION

Since the invention of Turing machine biological scientists have started using computational model for their biological computation. In this field there are lots of opportunities for research. There is still required to develop efficient tools/techniques for automatic DNA sequencing, protein structure prediction, obtaining phylogenetic tree, visualization tools, sequence analysis, etc.

Biological data are large in size, we need to deal with very large size sequences of DNA, RNA and protein, and therefore the problems in this area are generally found as computationally hard. Determining similarity between two sequences (i.e., obtaining pair wise alignment), among a family of sequences (i.e., multiple sequence alignment), classifying the members in different families according to their evolutionary distances and discovering the right ancestor of a candidate member will continue to be some of the most important and fundamental computational tasks. Some basic techniques for pair wise alignment can be seen in [16], [17]. Wang *et al.* describe techniques for DNA sequence classification tasks in [18].

VIII. AREA OF LANGUAGE PROCESSING

Language processing is a broad area that includes natural language processing, computational linguistics, and speech recognition, etc. This field always has been challenging for the scientists to work. Most of the time is spent for dealing with ambiguities. For example, the sentence "go to the bank" has ambiguity. Bank can be a financial bank, bank can be a river bank, bank can be a noun, bank can be a verb, etc. We expect the most probable meaning of this sentence which can be resolve by a particular context, past experience etc. machine needs to consider all possible contexts which may be infinite. Also past experience (database) should be processed as large as possible. The accuracy increases if we could process all possible contexts as well as reasonably large database. Therefore, for such computation computer requires large memory space and CPU time. This suggests that language processing seems to out of our practical reach. We need to determine tradeoff between accuracy and resource requirements.

There are good numbers of topics to choose as a line of work including resolving the ambiguity, parts of speech tagging, correcting spelling errors, determining the semantics, discourse

analysis which aims to determine the meaning of group of sentences instead of individual sentence or word processing, and speech recognition.

Guessing the next most probable word is a crucial subtask of speech recognition, and hand-writing recognition etc. There are number of language models can be seen in the literature including n-gram [19], [20].

The n-gram language model estimates the probability of a word, given previous words $(w_n|w_1, . . ., w_{n-1})$ where n is usually set to 2 (bigram), or 3 (trigram). The literal meaning of the word gram is token. The n-gram is a sequence of token in a given sentence. It is used to estimate the probability of a word occurring in n-1 context. It is used to model the syntax and semantics of natural language. An n-gram model relies on a Markov assumption that each word depends only on n-1 previous word. This works well with small training data. But, as training data size increases, language model size also increases, and then it becomes difficult to model the data for practical use.

A line of work is to find efficient language models for the word prediction and to evaluate their performance in order to positioning our work. To evaluate the performance of language models, we have various measures like Perplexity (PP), Word-Error-Rate (WER), and Relative Entropy (RE) [21].

Another important aspect in n-gram language modeling is smoothing to avoid zero probability estimations for unseen data. Various methods for smoothing techniques are developed so far. An interaction between pruning and smoothing can be seen in [22]. Further work is still required in the field of smoothing algorithm. In following we discuss two related areas that also seem to be promising.

A. Information Retrieval

Day by day knowledge (information) is increasing in exponential manner. Thus efficient management of such enormous documents becomes challenging. This makes the attention of research scientists to device scheme for storage of information and their subsequent retrieval. Information retrieval system depends on the way information is stored. It can be general, or for some specialized kinds of information. Vector space model is one of the information retrieval schemes where documents and queries are represented as vectors of features [23]. Features consist of terms that occur within the documents, with the value of each feature about presence or absence of given terms in a given document. So, information retrieval can be viewed as an optimization problem where objective is to obtain the document with respect to a given query where maximum numbers of terms are in common.

For evaluating an information retrieval system we need to know the notion of terms Recall and Precision [24]. These metrics we need to maximize. Recall is used to see the ability of system to retrieve relevant documents as follows:

$$\text{Recall} = \frac{No.\ of\ relevant\ documents\ returned}{Total\ no.\ of\ relevant\ documents\ in\ the\ collection}$$

Precision is a measure of accuracy of the system as given below:

$$\text{Precision} = \frac{No.\ of\ relevant\ documents\ returned}{No.\ of\ documents\ returned}$$

B. Machine Translation

The problem of translating from one language to another is known as machine translation (MT). We may require going for some or full process of MT depends on our need and application. If we have formal models for MT then many real problem including communication gap due to language barrier may be resolved. However, achieving full MT seems to be hard [24]. The MT process depends on the syntactical, morphological, semantic, and pragmatic structures of a particular language. So, we actually require developing efficient algorithms and data structures for handling the issues of natural languages. There are numbers of contributions have been done for MT using different methods including statistical approach. Some approaches can be seen in [25], [26], and [27].

IX. CONCLUSION

We have presented some selected research areas in theoretical computer science that we feel primarily important. We have also provided

important literatures that will be very useful for beginners to understand the field and to find the nature work needed in this area.

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PARALLEL ALGORITHM FOR ACCELERATING PATTERN MATCHING USING MPI

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Abstract— Pattern matching is a commonly used operation in many applications including image processing, bioinformatics, computer and network security, among many others. Knuth-Morris-Pratt (KMP) algorithm is one of the well-known pattern matching techniques and it is intensively used in computer and network security. Parallel algorithms for accelerating pattern matching have attracted a lot of attention due to their cost effectiveness and enormous power for massive data parallel computing. The proposed work of pattern matching is done using MPI on Intrusion Detection System (IDS) like Snort and the extracted pattern from Snort. Considering the parallel and distributed architecture, we proposed a method on which we perform very efficient parallel algorithm for KMP algorithm. The result shows the performance of parallel algorithm is completely outplayed the sequential performance using MPI.

Index Terms— Message passing Interface (MPI), Graphics processing units (GPU), pattern matching, parallel algorithm.

I. INTRODUCTION

Network Intrusion Detection System (NIDS) is widely used to protect computer systems from network attacks such as malware, port scans, and denial-of-service attacks. The most difficult part of NIDS is to inspect the packet content against the thousands of patterns. Because of that the increasing number of attacks, traditional sequential pattern matching algorithms is inadequate to meet the throughput requirements for high speed networks.

There were many approaches have been proposed to accelerate the pattern matching. The hardware approaches is classified into logic architecture [1], [2], [3], [4] In this architecture attack patterns are synthesized into logic circuits which are typically implemented on Field Programmable Gate Array (FPGA) to match more than one pattern in parallel. In comparison, memory architectures [5], [6], compile attack patterns into a state machine and perform pattern matching.

Recently, GPUs has been accepted to accelerate pattern matching because of their enormous power for massive data parallel computing. Wu-Manber-like multiple-pattern matching algorithm on GPUs achieved speedup two times as fast as the modified Wu-Manber algorithm used in Snort system.

The proposed work of pattern matching is done using MPI on IDS like Snort and the extracted pattern from Snort.

II. LITERATURE SURVEY

GPUs have been adopted to accelerate pattern matching because of their enormous power for massive data parallel computing. Pattern matching is widely used in various applications such as in Network intrusion Detection System (NIDS), cancer pattern, natural language processing, spam filter, word processor etc.

A. Naive Brute Force

It is one of the simplest algorithms which having complexity O (m n). In this, the First character of a pattern P with length m is aligned with the first character of text T with length n and then scanning is done from left to right after that shifting is done at each step it gives less efficiency.

B. *Boyer Moore Algorithm*

It performs larger shift-increment whenever there is a mismatch. It differs from Naive in the way of scanning. It scans the string from right to left; unlike Naive approach that is P is aligned with T such that the last character of P will be matched to first character of T. If character is matched, then the pointer is shifted to left to very rest of the characters of the pattern. If a mismatch is detected at say character c, in T which is not in P, then P is shifted right to m positions and P is aligned to the next character after c. If c is part of P, then P is shifted right, so that c is aligned with the rightmost occurrence of c in P. The worst complexity is still O (m + n).

C. *Knuth-Morris-Pratt (KMP)*

This algorithm is based on automaton theory. Firstly a finite state automata model M is being created for the given pattern.
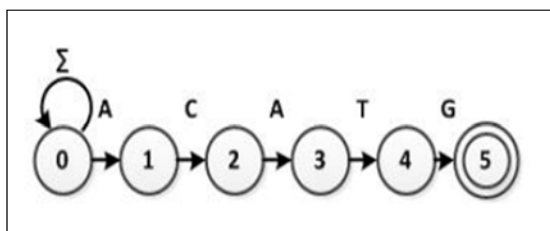

Fig.1 NFA for ACATG

The input string T with ∑ = {A, C, T, G} is processed through the model. If pattern is presented in the text, the text is accepted otherwise rejected. The following figure is a NFA model, created in ACATG string pattern.

The only drawback of the KMP algorithm is that it doesn't tell the number of occurrences of the pattern. The following Figure is the equivalent DFA of the above NFA.
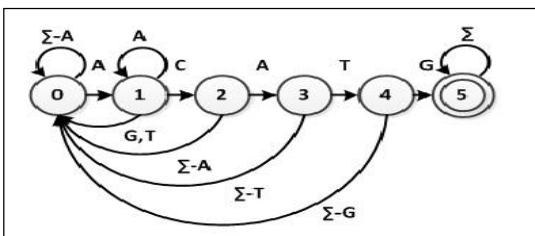

Fig. 2 Deterministic Finite Automata for ACATG

III. MESSAGE PASSING INTERFACE (MPI)

The aim of the MPI is to establish an efficient and flexible standard for message passing which is used for writing message passing programs. As such, MPI is the vendor independent and having message passing library. The benefit of developing message passing software using MPI helps to achieve design goals like portability, efficiency and flexibility. MPI performs their operations by using the methods such as MPI_send, MPI_receive, MPI_COMM_WORLD, MPI_Init and many more by Using these kind of functionality the processes communicate with themselves.

IV. PROPOSED WORK

The proposed work is dealing with the implementation of an efficient parallel algorithm for the pattern matching KMP algorithm [7]. The Naive pattern searching algorithm doesn't work well in the cases where we see matching characters followed by a mismatch.

The KMP matching algorithm uses degenerating property i.e. pattern having common sub-patterns appearing more than once in the pattern and it improves the worst case complexity to O (n). The idea behind KMP's algorithm is after some matches whenever we detect a mismatch, we already know that few of the characters in the text since they matched the patterns before the mismatched. Then by using this information we prevent matching characters that would be anyway going to match.

This algorithm usually does preprocessing over the pattern pat [] and it constructs an auxiliary array lps[] of size m which is the same as the size of the pattern. In this the lps stands for longest proper prefix which is also suffixed. For each sub-pattern pat[0..i] where i = 0 to m-1, lps[i] stores the length of the maximum matching proper prefix which is a suffix of the sub-pattern pat[0..i].

If the matching pattern is long the computation time gets increases to perform the matching and we are matching the multiple patterns in this paper.

V. PARALLEL IMPLEMENTATION OF KMP ALGORITHM

The steps of parallel implementations using MPI are given below:
1) Read the input file of Snort rules, prepare the input stream of that file, obtain the file size, allocate memory to contain whole file, copy the file into the buffer and divide it across processes using MPI_Bcast and MPI_Barrier.
2) Prepare the input stream of pattern file and get the number of lines.
3) Divide the input file among the processors.
4) Call the KMP search function and compute the longest proper suffix and at last show the matching patterns as output.

VI. RESULTS

The most time consuming part of KMP search is LPS that is Longest Prefix Suffix. The following results show the
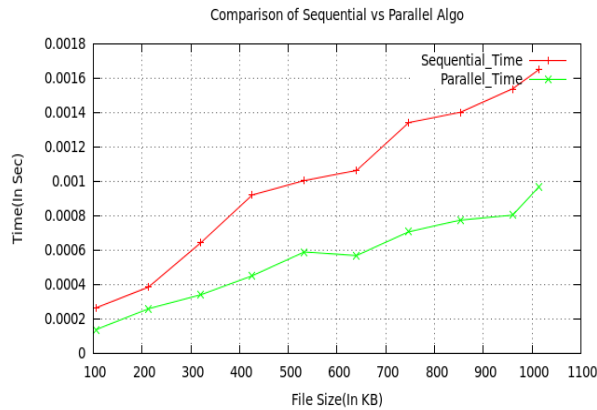Compute time of this algorithm.

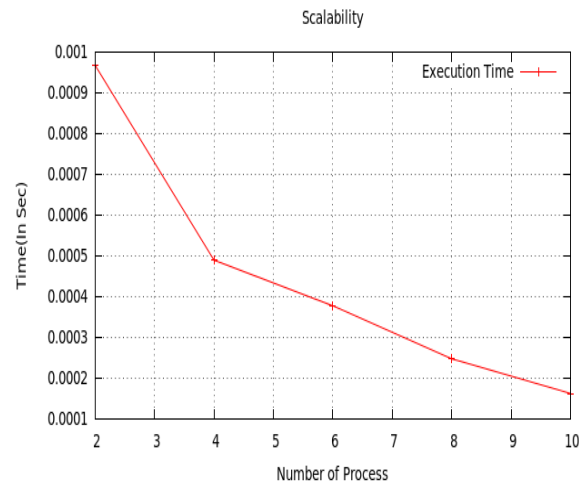Fig.3 Sequential Vs Parallel Time Comparison graph

Fig.4 Scalability

The above graph in fig. 3 shows the comparison of sequential and parallel time in which we have taken the input file in KB on X-axis and Time(s) to compute in Y-axis by keeping the pattern file constant. So the above graph shows that the parallel computation time is more efficient than the sequential time and the performance of parallel is completely outplayed the sequential performance.

The graph above in fig. 4 shows the number of processes on X-axis and the time taken by that process on Y-axis. In the above graph we have taken the 10 processes and computed the time taken by them in seconds. It shows that if we go on increasing the number of processes, then the performance gets better. In this way the scalability is achieved.

VII. CONCLUSION

In this project we have implemented the Knuth-Morris-Pratt algorithm to match the Snort pattern and the performance of the parallel algorithm is far better than the sequential algorithm for multiple patterns.

The future work would be to use this technique using CUDA (Compute Unified Device Architecture).

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REDUSING THE STORAGE SIZE USING COMPRESSION ALGORITHM AND CLOUD BACKUP USING EXOR

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Abstract – Cloud computing is a computing terminology based on utility and consumption of computing resources. It involves software networks and remote servers that allow centralized data storage and access to computer resources or services. In cloud computing we need to maintain data efficiently, hence there is a need of data recovery services. To achieve this we use seed block algorithm (SBA). The objective of proposed algorithm being, first to help the users to collect information from any remote location in the absence of network connectivity, second is to store data in compressed form and saving storage space, and third to recover the files in case of the file deletion or if the cloud gets destroyed due to any reason. The time related issues are also being solved by proposed SBA. Such that it will take minimum time for the recovery process. This algorithm also focuses on the security concept for the back-up files stored at remote server. we are also implementing compression algorithm to overcome the problem of storage size.
Keywords—Seed Block Algorithm, Remote Data Backup server (key words)

I. INTRODUCTION

The data files or information regarding clients which is stored in computer or laptop is lost due to hardware problem like if the system gets physically crashed or data gets corrupted, we are left with no other source to recover it. It is a very tedious job to manage various client records since work is done manually and there are a lot of chances made that create errors in maintaining the user account. Also there is a large data storage problem in the centralized system. Hence at times the data is lost from main server and there is no other backup facility to restore this data. This application provides a feasible solution that collects data and sends it to a centralized storage location smartly and we can access the data remotely.

Cloud computing is defined as a model for enabling convenient, on-demand network access to a shared pool of configurable computing service that can be provisioned rapidly and released with minimal management effort or services provider. In today's world, Cloud Computing itself is a gigantic technology which is surpassing all the previous technologies of computing in this competitive and challenging IT world. Its advantages overcome the disadvantage of various early computing techniques, increasing its demand day by day. Cloud storage provides online storage where data stored in form of virtualized pool that is usually hosted by third parties. The hosting company operates a large data on a large data centre. According to the requirements of the customer this data centre virtualizes the resources and exposes them as the storage pools that helps user to store files or data objects. As a number of users share the storage and other resources, it is possible that other customers might be able to access your data. Either the human error, faulty equipment's, network connectivity, a bug or any criminal intent may put our cloud storage at risk. Also changes in the cloud are also made very frequently; we can term it as data dynamics. The data dynamics is supported by

various operations such as insertion, deletion and block modification. Since services are not limited for archiving and taking backup of data, remote data integrity is also needed. The data integrity always focuses on the validity and fidelity of the complete state of the server that takes care of the heavily generated data which remains unchanged during storing at main cloud remote server and transmission. Integrity plays an important role in back-up and recovery services. However, various successful techniques are lagging behind some critical issues like cost, implementation complexity, security and time consumption. To cater these issues, we propose a smart remote data backup algorithm.

II. RELATED WORK

The recent back-up and recovery techniques that have been developed in cloud computing domain are HSDRT [2], (PCS) [3] Parity Cloud Service, (ERGOT) [4] Efficient Routing Grounded on Taxonomy, Linux Box [5], Cold/Hot backup strategy etc. Survey shows that none of these techniques are able to provide us with best performances under all uncontrolled circumstances such as cost, security, implementation complexity, redundancy and recovery in short span of time.

There are many techniques like HSDRT with many advantages like low cost privacy it has some disadvantage like implementation complexity was very high. Another technique is ERGOT which performs exact match retrieval but problem with this system is time complexity, implementation complexity. Linux box is also one of the technique to get the data backup but it requires Required higher bandwidth, Privacy is not provided, it takes Complete server backup at a time. in Cold/Hot Back-up Strategy there is problem when Cost increases as data increases gradually so to overcome all such problems we have introduced another technique using Seed Block Algorithm(SBA) for data recovery.

PCS has proved to be more convenient for data recovery based on parity recovery services. It is simple, more reliable and easy to use but is unable to control implementation complexities. On the other hand HSDRT has come out an efficacious technique for movable clients like laptops. But implementation of the recovery cost is high, also fails to control data duplication.

ERGOT is unable to focus on time and implementation complexity. However, Linux Box model provides data backup and recovery at a comparatively low cost but its protection level is very low.

The table below shows the comparison of these techniques,

III. NEED FOR BACK-UP IN CLOUD COMPUTING

Cloud computing provides on demand resources to the consumer/user. It requires management of resources among every client/user accounts. Such management includes various aspects of proper utilization of the resources. The resources can be any hardware or software, software like any application development kit, application programming interface or a type of data file. There are various choices among various implementations for back up of the data that maintain its security among various users. Cloud computing must be able to provide reliability such that users can upload their sensitive and important data which is kept secure. Also, implementation of this system over a large scale leads to an enormous amount of data being stored on the server. To deal with this efficiently, the data needs to be stored in compressed for so as to save storage space. The cost-effective approach is the main concern while implementing any cloud.

During the study of cloud computing, we found various advantages of cloud computing. It is found that the cloud is capable enough to store huge amount of data of various different clients with complete security. This enables the Internet Service Provider (ISP) to provide a huge storage in a cloud to the user. The users are allowed to upload their private and important data to the main cloud. At the same time we found a critical issue regarding storage i.e. if any of the client's data file is missing or disappears for some reason or the cloud gets destroyed either due to any natural calamity (like flood, earthquake etc.), then for back-up and recovery consumer/client has to depend on service provider which means the data has to be stored in the server.

To overcome this problem, it requires an efficient technique for data backup and recovery so that the client is able to contact the

backup server where private data is stored with high reliability whenever a main cloud fails to provide the user's data. These techniques must be provided at low cost as well as for implementation of the recovery problem's solution, it should be easy to recover the data after any disaster. Due to heavy storage of the clients, the need of back-up and recovery techniques in cloud computing arises.

A. Problem Statement

In cloud computing, to maintain the data efficiently, there is a necessity of data recovery services. To cater this, we propose a smart remote data backup algorithm, Seed Block Algorithm. Using Seed block algorithm we recover the files in case of the file deletion or if the cloud gets destroyed due to any reason. The time related issues are also being solved by proposed Seed Block Algorithm such that it will take minimum time for the recovery process. Proposed algorithm also focuses on the security concept for the back-up files stored at remote server, without using any of the existing encryption techniques.

The objective of proposed algorithm to help the users to collect information from any remote location, to store data in the cloud in compressed form to save space and to recover the files in case of the file deletion or if the cloud gets destroyed due to any reason. Usually Backup server of main cloud is the copy of main cloud. When this Backup Server is at remote location (i.e. far away from the main server) and has the complete state of the main cloud, this remote location server is termed as Remote Data Backup Server. The main cloud is termed as the central repository and remote backup cloud is termed as remote repository. To tackle the challenges like low implementation complexity, low cost, security and time related issues we propose Seed Block Algorithm.

IV. REMOTE DATA BACK-UP SERVERS

Remote Data Backup server is a server which stores the main cloud's entire data as a whole and located at remote place (far away from cloud). There are an anormous number of users using the storage space. Hence, we compress the data when it is being stored in the backup server. This helps us use the least amount of storage space. If the central repository loses its

data, it uses the information from the remote repository. The purpose is to help clients to collect information from remote repository if the main cloud is unable to provide the data to the clients. As shown in Fig 1, if clients found that data is not available on central repository, then clients are allowed to access the files from remote repository (i.e. indirectly).
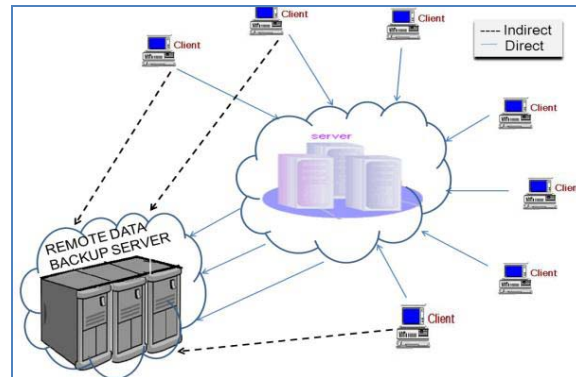

Fig. 1. Remote data Backup Server and its Architecture

V. SBA - ALGORITHM IMPLEMENTATION

The proposed SBA algorithm is as follows:
Algorithm 1:
The proposed SBA algorithm is as follows:
Algorithm 1: Initialization: Main Cloud: Cm:
Remote Server: Rs;
Clients of Main Cloud: Cn; Files: f1 and f1';
Seed block: Sb; Random Number:
Rn ; Client ID:Cilent-Idi
Input: f1 created by Cn; Rn is generated at Cm;
Output: Recovered file f1 after deletion at Cm
Given: Authenticated clients could allow uploading, downloading and do mod-
ification on its own the files only.
Step 1: Generate a random number.
Int Rn=rand ();
Step 2: Create a seed Block Sb for each Cn and Store
Sb at Rs
Sb = Rn EXOR Cilent-Idi (Repeat step 2 for all clients)
Step 3: If Cn/Admin creates/modifies f1 and stores at
Cm, then create as f1'
f1'= f1 EXOR Sb
Step 4: Store a at Rs
Step 5: If server crashes f1 deleted from Cm
Then we do EXOR to retrieve the original f1 as:

f1= f1' EXOR Sb
Step 6: Return f1 to Cn
Step 7: END

Since a backup system contains at least one copy of all data worth saving, the data storage requirements can be significant. Organizing this storage space and managing the backup process can be a complicated undertaking. Hence we compress the data that is being stored in the backup server saving up most of the space. A data repository model can be used to provide structure to the storage. Nowadays, there are many different types of data storage devices that are useful for making backups. The Remote backup services should cover the following issues:

- Privacy and ownership.
- Relocation of servers to the cloud
- Data security
- Reliability
- Storage space management
- Cost effectiveness
- Appropriate Timing

Privacy and ownership:
Different clients access the cloud with their different login or after any authentication process. They are freely allowed to upload their private and essential data on the cloud. Hence, the privacy and ownership of data should be maintained; Owner of the data should only be able to access his private data and perform read, write or any other operation. Remote Server must maintain this Privacy and ownership.

Relocation of server:
For data recovery there must be relocation of server to the cloud. The Relocation of server means to transfer main server's data to another server; however the new of location is unknown to the client. The clients get the data in same way as before without any intimation of relocation of main server, such that it provides the location transparency of relocated server to the clients and other third party while data is been shifted to remote server.

Data security:
The client's data is stored at central repository with complete protection. Such a security should be followed in its remote repository as well. In remote repository, the data should be fully protected such that no access and harm can be made to the remote cloud's data either intentionally or unintentionally by third party or any other client.

Reliability:
The remote cloud must possess the reliability characteristics. Because in cloud computing the main cloud stores the complete data and each client is dependent on the main cloud for each and every little amount of data; therefore the cloud and remote backup cloud must play a trustworthy role. That means, both the server must be able to provide the data to the client immediately whenever they required either from main cloud or remote server.

Storage space management:
The data a client/user uploads gets stored on the cloud. The number of users using the cloud is large, so is the amount of data being stored in the cloud. To use the resources effectively, we compress this data at the storage. This saves up a lot of space for other data to be stored.

Cost effectiveness:
The cost for implementation of remote server and its recovery & back-up technique also play an important role while creating the structure for main cloud and its correspondent remote cloud. The cost for establishing the remote setup and for implementing its technique must be minimum such that small business can afford such system and large business can spend minimum cost as possible.

Appropriate Timing:
The process of data recovery takes some time for retrieval of data from remote repository as this remote repository is far away from the main cloud and its clients. Therefore, the time taken for such a retrieval must be minimum as possible such that the client can get the data as soon as possible without concerning the fact that remote repository is how far away from the client. There are many techniques that have focused on these issues. In forthcoming section, we will be discussing some of recent techniques of back-up and recovery in cloud computing domain.
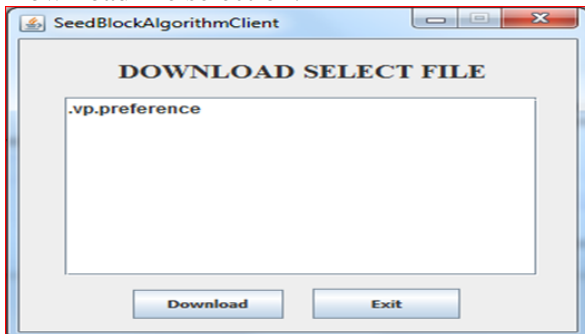
VI. RESULTS

Registration:

File upload/download:
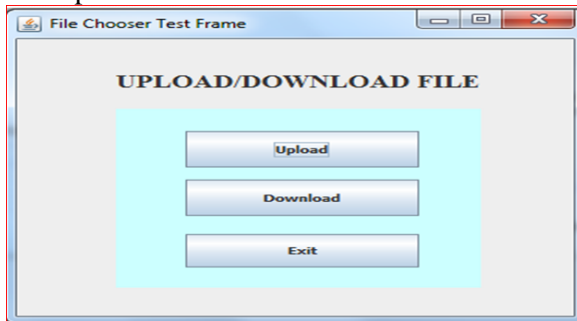
Download file selection:

CONCLUTION

This implementation paper proposes a technique to perform a smart remote data backup using SEED Block Algorithm. The Seed Block Algorithm is time efficient technique to recover lost files. It maintains the data integrity and solves the issues like cost, implementation complexity, data storage. SBA also focuses on the security concept for the back-up files stored at remote backup server.

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PRIMARY DESIGN AND DEVELOPMENT OF EGR SYSTEM FOR COMPUTERISED SINGLE CYLINDER FOUR STROKE DIESEL ENGINE

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Abstract: **The aim of present work is to study effect of exhaust gas recirculation system on engine performance and emission. EGR system is designed and then fabricated by considering specification of engine. Single cylinder four stroke computerised diesel engine is selected for design. Theoretical study is carried out to design EGR system. At successful completion of design work it is expected that developed EGR system will work effectively.**
Keywords— **EGR system, engine performance, emission**

1. Introduction
The Theory of compressed-ignition (CI) Engines is developed by Rudolf Diesel. The survey of CI engine application it is found that there is challenge to increases engine performance and reduces emission from the engine. As we know that CI Engines are better power source due to higher compression ratio, higher efficiency, performance, and reliability than SI Engines. Hence, in most of on-road transportation, and off- road stationary applications, CI Engines are widely used . Exhaust gas from the engine is re-circulated by using outside bypass provided. Exhaust gas having capability of absorbing oxygen content from the air because of these combustion flame temperature is decreases. EGR is to reduce NOx by decreasing oxygen content and combustion flame temperature.

Some researcher had concentrated on this technique which reduces emission from the engine. N.V. Deshpande et al.(2008) had given emphasis to control oxides of nitrogen (NOx). He reported the effect of EGR rate on NOx, smoke, and on performance parameter like BSFC, and brake thermal efficiency etc. He was found that with increasing rate of EGR for different torque there was marginal decrease in brake thermal efficiency. This was due oxygen deficiency at higher load, which lead to incomplete combustion. In addition, BSFC was also marginally increased at high load.

A.K. Agrawal et al.(2004). worked out an experimental investigation to observe effect of EGR on exhaust gas temperature and exhaust opacity in CI Engines. He was observed that, as EGR rate increases exhaust gas temperature decreases significantly. However, this result surely concludes that NOx can be decreased by increasing EGR rate. The reason for decreasing exhaust gas temperature was stated as considerable decrease in oxygen content in recirculation of exhaust gas to fresh air/charge.

Timothy Jacobo et al.(2003) investigated that, the coupling between EGR, the variable geometry turbo-charging (VGT), and EGR cooler critically affects boost pressure, air/fuel ratio (A/F), combustion efficiency and pumping work. Engine thermal efficiency tends to decrease with EGR rate.

M. Ghazikhani et al. (2010)carried out an experimental study to investigate effect of EGR on various exergy terms of IDI diesel engine cylinder. In this study, also the effectiveness of total in-cylinder irreversibility on brake specific fuel consumption (BSFC) was investigated.

Alain Maiboom et al.(2009) studied the influence of cylinder-to-cylinder variations in EGR

distribution on the resulting NOx–PM trade-off had been experimentally investigated on an automotive high-speed direct injection Diesel engine. It was reported that, Unequal EGR distribution results in increased NOx and PM emissions compared to engine running with well mixed air and EGR gases. Furthermore, the increase in emissions was due to cylinder-to-cylinder variations in both gas composition and intake temperature. He was also concluded that, the suppression of unequal cylinder-to-cylinder EGR distribution results in a large reduction of NOx and PM emissions, especially when running with high EGR rates. An optimized air–EGR connection will be one of the ways to achieve future emissions standards.

2.Expremental Set up

Single cylinder four stroke computerised diesel engine is selected. Computer can be used for the control of a test and data acquisition, thus improving the efficiency of engine testing. The computer can also process all data, carry out statistical analysis, and plot all the result. Engine Soft is useful for testing and analysing performance of various parameter of engine.EGR system is designed and then fabricated by considering specification of engine. There are two type of EGR system by considering temperature, first is hot EGR system, in this system hot gasses is directly recalculated in the engine and second is cold EGR system, in this exhaust gasses is cooled by using EGR cooler. Cold EGR system is more effective than hot EGR system. Fig1. show that photograph of computerised single cylinder four stroke engine without installing EGR system. Brief specifications of engine are given below. Moreover, all tests will be conducted and parameters will be measured under steady state operation.

a) Specification of engine

Manufacturer - Kirloskar oil engine Ltd, Pune. Single cylinder four stroke diesel engine. Cubic capacity - 661 cc Bore - 87.5 mm-110 mm Cooling system- Water Power- 7 hP @ 1500 rpm.
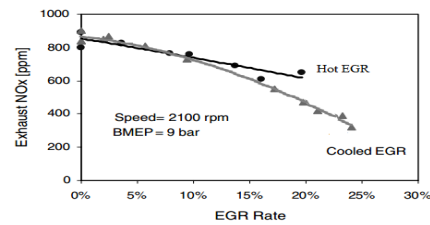

Fig1. Engine set up without EGR system

Fig 2. Comparison between cooled and hot

EGR[Zing M et al 2004].

The EGR system will fabricated as per requirements. The set-up will then, modified by incorporating exhaust gas recirculation sub-system in the set-up as shown in Fig. 3. A short cooled EGR system will chosen for study due to its merits.

b) Various Instruments and Measuring Devices

i)Load and Speed Measurements

The engine will directly coupled to an eddy current dynamometer that permitted engine motoring fully or partially. The engine and dynamometer were interfaced to a control panel. A photo sensor along with a digital rpm indicator will used to measure the speed of the engine. The voltage pulses from the sensor are sent to the digital rpm meter for pulse conversion and display of the engine speed with an accuracy of 1 rev/min.

ii) Air Flow Measurement

Airflow rate will measured using air box method.

iii)The Fuel Supply and Measurement

Supply of fuel will done through a fuel tank placed at over head of M.S framed stand. The supply of fuel to fuel pump will done through three will solenoid valve. One will connection will taken fuel from tank while of the other two connections one will given to burette and remaining will connected to fuel pump filter.

This will so to measure fuel consumption of engine by closing valve of fuel tank line to restrict fuel from fuel tank allowing fuel consumption only from measuring burette.

iv)Temperature Measurement

Temperature of the exhaust gas will measured with thermocouples. A digital indicator with automatic room temperature compensation facility will used. The temperature indicator will calibrated periodically.

v)Pressure Measurement

In cylinder pressure will measured with a water-cooled piezoelectric transducer. The pressure pick up will mounted on to the cylinder head surface. A PCB Piezotronics make transducer with a sensitivity of 0.145mV/kPa will used for the purpose. A piezoelectric transducer produces a charge output, which is proportional to the in-cylinder pressure.

Fig 3. Engine fitted with EGR system

c) The necessary components for EGR set-up fittings are
 i)Calorimeter ii)EGR Cooler iii) EGR Valve iv)Gas Pipe connection v)Control Valve

i) Calorimeter

Pipe in pipe type calorimeter is selected which is used to reduce the temperature of hot gasses

ii) EGR cooler

Shell and tube type heat exchanger is selected because it is operated with high temperature and pressure. It consist of Shell, round aligned type tube and baffles. Baffles are placed at equidistance from each other. Total length of Cooler is 600 mm. Flow arrangement is selected is counter flow because high rate of heat transfer.

iii) EGR Valve

Exhaust gas from the engine is again recalculated with help gas route pipe. Exhaust gas controlled by using EGR valve. It is operated with manually.

$$\% \text{ EGR} = \frac{M_{EGR}}{M_{Total\ Intake}} \times 100$$

However, mass of re-circulated exhaust gas will calculated based on difference in manometer column for consecutive revolution (position) of EGR valve. For respective EGR valve position decrease in difference in manometer column will observed compared to (without EGR) total intake charge suction. This decrease in column is nothing but mass of exhaust gas re-circulated during respective valve position. Therefore, this value of mass of exhaust gas re-circulated will determined. We have the total suction during without EGR. This interprets rate of EGR circulated. If EGR valve is totally closed no exhaust gas is circulated. Material of valve is withstand with high temperature and pressure.

iv)Control Valve

Control valve is used to control flow rate of exhaust gasses. if any back pressure is there then open the control valve so that engine operated smoothly.

v)Gas pipe connection

Material used for gas pipe connection is GI. Diameter of pipe is 2 inch. T connection of pipe consist of recirculated exhaust gasses, fresh air from air box and connected to intake manifold.

Table 1. Specification of exhaust gas recirculation system

Sr.No	Component	Specification
1	EGR cooler	Shell and tube
2	Type of flow	Counter flow
3	Shell fluid	Water (coolant)
4	Tube Fluid	Gas
5	Core length	600 mm
6	Shell diameter	150 mm
7	EGR valve (Gate valve)	Manually operated
8	Gas pipe GI	2 inch.
9	Control valve	Manually operated

Conclusion

From this Work getting the idea about selection of various parameter for EGR system. Cold EGR system is selected due to its merit. Based on theoretical design consideration, EGR system is fabricated. After installation of this system on the single cylinder four stroke computerised diesel engine various experimental test will be

conducted and engine performance will be checked with or without EGR system.

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ANALYSIS OF SPUR GEAR GEOMETRY AND STRENGTH WITH KISSSOFT SOFTWARE

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Abstract- **Transmission is usually very complex with a lot of gear pairs, shafts and bearings in it. Modern transmissions have also several functionalities like shifting without clutch, 4WD/2WD, forward and reverse shuttle and Power take off units. They must work smoothly and quietly like an automotive transmission, but usually working conditions are much more severe. They must also be reliable in different kind of working conditions and fields of applications. Because of the great variety of gears and speeds selectable, calculations for safety factors and component lifetimes becomes usually very complex, time consuming and challenging to manage. This paper describes the parameters to be considered while designing gear pair in KISSsoft software. KISSsoft provides calculation for different toothing types, ranging from cylindrical gears in different configurations**
Keywords- KISSsoft software, Gear pairs

Introduction

All vehicles require transmissions in order to convert torque and engine speed. The most powerful engine in the world is of little use unless the power from the engine can be safely and effectively transmitted to the ground. In addition to being able to transmit the torque and power from the engine, the transmission and driveline also must allow the vehicle to operate over a wide range of speeds-from a standstill to the maximum speed of the vehicle. This implies that the system must inherently have some method of disconnecting the engine from the remainder of the driveline to allow the vehicle to remain stationary. The transmission must be designed to satisfy the conflicting requirements of quick acceleration, high speed, and adequate fuel economy. Transmissions are distinguished in accordance with their function and purpose Gears are the most common means of transmitting power in the modern mechanical engineering world. Spur gear are the most common type of gear used for transmitting power between two parallel shafts. Spur gear have their own advantages like they have high power transmission efficiency, have constant velocity ratio, highly reliable and easy to install so it is necessary to check spur gear geometry and strength.

2. The KISSsoft input parameters and analysis of gearbox elements

KISSsoft is a software package for calculating machine elements. While gears are a natural focal point, owed to their central role in transmission, the software also covers shafts, bearings, connecting elements, springs, belts and others. Gears calculations cover all

common gear types: cylindrical gears, bevel gears, worm gears, helical gears, hypoid gears and face gears, for cylindrical gears also as planetary sets and gear racks. In addition to the strength analysis according to the respective standards (ISO, AGMA, DIN), the program also offers a number of different design and optimization functions and methods exceeding the standards. And of course all important geometry calculations are carried out, control measures for the manufacturing are provided and the tooth shape is represented in two and three dimensions. Using current standards as its basis, KISSsoft serves as an easy and safe tool for verifying the strength of cylindrical gears and offers a number of different methods. The software calculates resistance to pitting, scoring and breakage at the root of a gear tooth, and, if given a minimum safety factor, can also determine transmittable power and achievable service life. Geometry calculations provide all relevant dimensions and test measures based on applicable standards and under full consideration of relevant tolerances. The pre-sizing feature provides a series of suggestions for gear pairs aimed at solving a transmission problem. On the one hand, this step provides reasonable ranges for the module, centre distance, face width and number of teeth; on the other hand, the concrete solution also serves as a starting point for further optimization work. For cylindrical gears the fine sizing feature, which combs through entire ranges of parameters and validates solutions based on a variety of criteria, offers a powerful tool to find the optimal solution. CAD interfaces allow the user to represent a gear in two-dimensional format as a DXF or IGES file.

Fig.1. Basic data input window for cylindrical gear pair

The Basic data input window is one of the standard tabs and is subdivided into the two groups Geometry, Material and Lubrication.

a. Normal module
The normal module defines the size of the teeth. A standard series is for example defined in DIN 780 or ISO 54. However pitch is known, the transverse module or the diametral pitch instead of the normal module, click the button to open a dialog window in which the conversion will be performed and to transfer the diametral pitch instead of the normal module, select Input normal diametral pitch instead of normal module by selecting Calculation > Settings > General.

b. Pressure angle at normal section
The normal pressure angle at the reference circle is also the flank angle of the reference profile. For standard toothing the pressure angle is $\alpha_n = 20°$. Smaller pressure angles can be used for larger numbers of teeth to achieve higher contact ratios and insensitivity to changes in centre distance. Larger pressure angles increase the strength and allow a smaller number of teeth to be used without undercut. In this situation, the contact ratio decreases and the radial forces increase.

c. Centre distance
As stated in ISO 21771, the axis center distance for external and internal gears is positive for two external gears and positive for an external gear paired with an internal gear. For internal teeth, the number of teeth on the internal gear and the axis center distance are always negative. If checkbox to the right of the axis center distance unit is selected, the value used in the calculation will remain constant. Otherwise, the axis center distance will be calculated from the profile shift total.

d. Number of teeth
The number of teeth is, by default, a whole number. For internal toothed gears, you must enter the number of teeth as a negative value as stated in ISO 21771. For a pinion-ring internal

gear pair, the center distance must also be entered as a negative value The minimum number of teeth is limited by geometric errors such as undercut or tooth thickness at the tip. For spur gears without profile shift there is for example undercut if there are fewer than 17 teeth

e. Face width
Normally the face width shouldn't be greater than 10 to 20 times the normal module, or also not greater than the reference circle of the pinion. The contact pattern deteriorates if the face width is too great. The common width is used to calculate the pressure. A certain amount of overhang is taken into account for the Tooth root strength. The selected pinion width is often somewhat greater than the gear width.

f. Geometry details
To open the Define geometry details window, click the Details button in the upper right-hand part of the Geometry area.
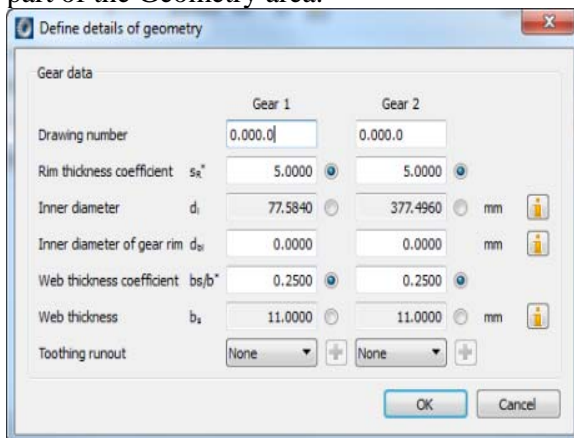

Fig.2. Geometry details for cylindrical gear pair

Values like Drawing number, Rim thickness coefficient , Inside diameter, Inside diameter of rim, Web thickness coefficient , Web thickness can be changed. The drawing number is only used for documentation purposes. The inside diameter is needed to calculate the mass moment of inertia. In accordance with ISO or AGMA, the gear rim thickness, defined by the inside diameter of rim, affects the strength. If no gear rim thickness is present, enter a value of 0.

In this case the gear rim thickness will be determined.

g. Service life
Enter the required service life directly in the input field. Based upon the minimum safety value for the tooth root and flank strength, this process calculates the service life (in hours) for every specified gear and for every load. The service life is calculated in accordance with ISO 6336-6:2006 using the Palmgren-Miner Rule. The system service life and the minimum service life of all the gears used in the configuration is displayed.

h. Application factor
The application factor compensates for any uncertainties in loads and impacts. When deciding which application factor should be selected, you must take into account the required safety values, assumed loads and application factor in one context..

3. Calculation method
In the drop-down list, various calculation methods can be selected as follows :

a. Geometry calculation only
If the Rating module is not selected in the Calculation menu, only the geometry is calculated.

b. Static calculation
In a static calculation, the nominal stress is usually compared with the permitted material parameters like yield point and/or tensile strength. This runs a static calculation of cylindrical gears in KISSsoft where the nominal stress in the tooth root which is calculated by tooth form factor YF and compared with the yield point and tensile strength. Each coefficient such as application factor, face load factor, transverse coefficient, dynamic factor is set to 1.0. The load at the tooth root is calculated in accordance with ISO 6336 method B with the tooth form and the helix angle without the stress correction factor.

c. AGMA 2001-C95

This edition of the AGMA 2001-C95 American national calculation guideline replaces AGMA 2001-B88. However, the new edition does include the service factor calculation. The standard is implemented in its complete form and the dynamic factor and the face load factor are calculated in accordance with AGMA recommendations. The geometry factors (for tooth root and flank) are calculated entirely in accordance with ANSI/AGMA 908-B89. In addition to all the relevant intermediate results, the following values are also supplied: Pitting Resistance Power Rating, Contact Load Factor, Bending Strength Power Rating, Unit Load for Bending Strength, Service Factor. This calculation can also be used for every other cylindrical gear configuration including planetary stages. However, it is remarkable that AGMA Standards do not permit the direct calculation of tooth root strength in internal gear pairs. In this case the calculation must be performed using the graphical method

4. Theoretical Safety Factors

As with every gear, a validation of the strength is given as safety factors for pitting and root strength. In order to evaluate these factors, it is important to know the minimal required values. This is a general problem associated with machine construction. Minimum safety values can be very different, and should be determined most of all on the basis of experience and proven results from a test rig. In cases where nothing similar is known, the following values can be used as a starting point:

Minimum root safety factor : 1.4

Minimum flank safety factor : 1.0

These factors are impressively low. The gear used was a ground face gear of very high precision. The face load co-efficient chosen in this case was set much too high. A validation through ISO 10300 with these factor gives a flank safety factor of 1.0, and root safety factor of 0.80. The flank safety factor corresponds roughly to expectation, but the root safety is so low that a break in the root can be expected.

4. Conclusion

The spur gears are simplest tooth elements offering maximum precision so recommended for all the gear meshes, except where very high speeds and loads or special features of other types, such as right angle drive. The availability of software for sizing spur gears and their associated tooling, it is now possible to efficiently overcome special calculation and manufacturing problems associated with tooth forms of this type in arriving at a practical, alternative solution. In this paper we have gone through pre-processor phase, where along with pre processing the geometry of the structure, the constraints, loads and mechanical properties of the gear pairs are defined. This paper describes about how spur gear pair is modeled in KISSsoft calculation software which is useful for final design of transmission.

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STUDY ON VIBRATION ANALYSIS OF COMPOSITE PLATE

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Abstract— As we all know that vibration and composite material are two main growing research topics these days. Almost all the structural components subjected to dynamic loading in their working life and vibration affects the working life of the structure so it is very important in designing a structure to know in advance its response and to take necessary steps to control the structural vibration and its amplitude. Composite material gives chances to designers and engineers to increase material efficiency, therefore resulting in cost reduction and better utilization of resources. Composites materials applications are wide in aerospace industries, automobile sector, manufacturing industries etc.

The present study involves extensive experimental works to investigate the free vibration of woven E-fiber Glass/Epoxy composite plates in fix-free boundary conditions. The specimens of woven E-glass fiber and epoxy matrix composite plates are manufactured by the hand-lay-up technique which is most suitable and efficient manufacturing technique for composite manufacturing. Elastic properties of the plate are also determined experimentally by tensile testing of specimens using computerized universal testing machine TUE-C-400. ASTM standard was used to test the material. An experimental investigation is carried out using modal analysis technique with VA4Pro FFT Analyzer, impact hammer and contact accelerometer obtain the Frequency Response

Functions. Also, this experiment is used to validate the results obtained from the ANSYS 15.0 and theoretical calculations based on governing equation of vibration. The effects of different geometrical parameters including number of layers, aspect ratio of woven E-glass fiber composite plates are studied in fix-free boundary conditions in details. This study provides valuable information for researchers and engineers in design applications.

Index Terms— Composite material, vibration, Modal analysis, finite element analysis, FFT analyzer, Fixed-free Boundary condition.

I. INTRODUCTION

Literature review focuses on the different types of analysis of composite materials. The basically composite material is a combination of two or more numbers of materials. It is simply made by putting several materials together and creating a product that is stronger than the sum of their materials. History of advance composites begins in 1970s in aerospace industries, but nowadays after only four decades, it is developed in most of the industries. There is possibility that increase in composite material characteristics using the latest technology and various manufacturing methods has raised its application range. Along with progress in technology, metallic parts are replaced by composite materials in various industries. In many cases materials encounter vibrations in

machines and mechanisms. The effect of vibration is very prominent whether it is small in amplitude or large. Considering the aero plane wings the effect of vibration can be severe as those are flexible structures. Due to the effect of vibration, strain in the wings increases. This can cause instability. To make the structure more flexible without compromising its strength, vibration study is very important. But still the effect of vibration could not be minimized to satisfy level.

In this paper work, basically vibration analysis of E-glass and epoxy composite plate was studied in which we analyzed the effect of factors such as number of E-glass fiber layers in composite material and an aspect ratio of reinforcement and matrix material by weight which was E-glass fiber and Epoxy on the fundamental natural frequency. Lots of researchers did their work on free-free boundary condition. This research totally focuses on the fix-free boundary conditions. Fix-free boundary conditions same as that of cantilever object boundary conditions. Rather than fundamental natural frequency we found different mode shapes of vibrations experimentally and analytically in this research.

The scope of the study includes below important points:

- Fabrication of E-Glass/Epoxy composite plate according to research requirement.
- Experimental Modal analysis work conducted on FFT analyzer and also on ANSYS.
- Aspect ratio and Number of layers were the affecting parameters of this experiment.

II. METHODOLOGY

In this research work, it was very important and necessary to develop proper composite plate and fabrication method to manufacture those plates. There are lots of fabrication methods to develop composite plate. It is essential for the reader to know how these processes. The selection of a fabrication process obviously depends on the constituent materials in the composite; with the matrix material is the dominant factor. Selection of reinforcement material also plays important role in the selection of manufacturing method. The name of fabrication processes given below:-

1. Hand lay-up.

2. Spray-up.
3. Automated lay-up.
4. Pultrusion process.
5. Filament winding.
6. Resin transfer molding.

Hand lay-up method was used to fabricate composite plate which was best suited for manufacturing those plates. Perfect plan is necessary to achieve good results to perform research. Simulation is carried out using analysis software ANSYS 15.0. FRF result, simulation results and theoretical results were compared. Methodology is a brief description about experimentation of the research.

A) Experimentation

a) Geometric properties: Woven E-glass fiber composite plates were taken as a specimen to conduct a test. The numbers of plates were taken. Plates prepared by hand lay-up by placing various layers of glass fiber on each other. The maximum length of plate is 25 cm. Plate widths and length remains constant throughout the research. The average thickness of the specimen was measured by a screw gauge having at L.C. Of 0.01mm.

b) Fabrication Method: Wet lay-up and autoclave is two important techniques to be considered for fabrication of composite materials. The hand lay up or wet lay-up processing techniques and autoclave techniques, processes have one thing in common: The deposition of different layer is done by hand. The most common materials are E-glass fiber and polyester resin, although higher performance materials can also be used. The single sided mold invariably operates at room temperature using an ambient curing resin. The reinforcement may be in the form of chopped strand mat or an aligned fabric such as woven roving's. The usual feature of hand laminating is a single sided female mold, which is often itself made of glass fiber reinforced plastics (GRP), by taking a reversal from a male pattern. The GRP shell is often stiffened with local reinforcement, a wooden frame or light steel work to make it. The mold surface needs to be smooth enough to give an acceptable surface finish and release

properties and this is provided with a tooling gel coat that is subsequently coated with a release agent. The latter prevents the matrix resin from bonding to the mold surface and facilitates the de-molding operation. It is common practice to use a surface tissue immediately after the gel coat to mask any reinforcement print-through on the outer surface. Once the gel coat has hardened sufficiently, the reinforcement is laid in one layer at a time. Catalyzed resin is then worked into the reinforcement using a brush or roller. This process is repeated for each layer of reinforcement until the required thickness is built up. For thick laminates, pauses need to be taken after a certain number of layers have been deposited to allow the exothermic heat to dissipate before additional layers are deposited. Local reinforcements can be used to provide stiffness in specific areas and lightweight formers such as foams or hollow sections can be laminated in for the same purpose. The process remains an important one for low volume manufacture, although increasingly stringent emission regulations are forcing several manufacturers to explore the use of closed mold alternatives.

We use E-fiberglass as a layer of the composite and epoxy as a binder to create hard composite materials. The percentage of fiber and matrix was 50:50 in weight at first, which will vary afterwards according to experiments. Below figure 1 shows the hand lay-up techniques.
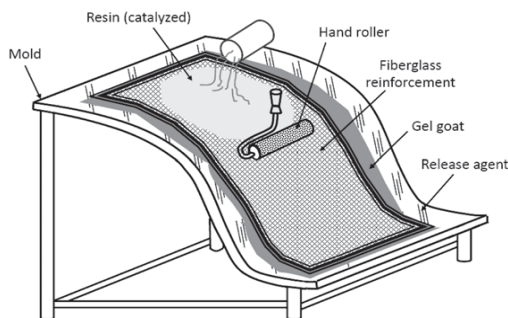

Fig. 1: Wet / Hand lay-up Fabrication process[16].

c) Determination of Material Constant: The fibers used in modern composites has strengths and stiffness's far above those of traditional bulk materials. The characteristics of woven E-fiberglass/epoxy composite plate which can be determined completely by two material constants E and ν. A composite plate according to experiment variations was manufactured to evaluate material constant. The constants E determined experimentally by performing tensile test on specimen as described in ASTM standard D-638. The specimen of same size plates was cut themselves by diamond cutter or by any cutting machine. After cutting in the cutting machine, it was polished in the polishing machine. At least three specimens were tested and mean value adapted. ρ also required for the simulation in ANSYS. This can be determined by measuring the mass of the plate divided by the volume of that plate. We took the average value for ν from the manufacturer's catalogue which was 0.275.

III. TESTING

FFT analyzer is used to analyze vibration in the specimen of having fix-free boundary condition. The instrument which converts the input signals, with time as an independent variable, into frequency spectrum and displays it in graphical form is called as spectrum analyzer or FFT analyzer.

A) Test Setup
Instruments: Following instruments used to perform the experiment:
- Impact Hammer.
- Accelerometer.
- Multi-channel Vibration Analyzer (At least two-channel).
- A PC/Laptop loaded with software for modal analysis.
- Test-specimen (A cantilever held in a fixture).
- Power supply for the instruments and vibration analyzer, connecting cables for the impact hammer and accelerometer, fasteners and spanner to fix the specimen

in the fixture, and adhesive/wax to fix the accelerometer).

The connections of all the instruments are done as per the guidance manual. The plate was excited by the impact hammer when the plate was in a fix-free condition. C-clamp required for holding the plate according to boundary conditions. Additional 5cm provided at the end of the plate for the hold.

B)Test Procedure

- Prepare the plate: Measure the length of the fixture that holds the composite plate and leave the margin of that length on the plate. Divide the remaining length of plate into five parts and mark node numbers in each division – from 1 to 6. Let node 1was the fixed end. Fix the accelerometer to the plate at node 3 but on the face of the plate opposite to the marking and node number up. Fix the plate into the C-clamp that provide support to the cantilever plate.

Fig. 2: Experimental setup

- Connect the wires and cables.
- Switch on the power supply. Open the software of vibration analysis and experimental modal analysis installed on the PC/laptop. Provide essential inputs and make necessary settings in the software. Ensure that there is proper supply and communication between the devices connected.

Now we shall provide impacts by the impact hammer on the nodes marked on the cantilever plate one by one. Impacts will be given with nodes 1, 2, 4, 5 and 6; node 1 is fixed and node 6 is free. The accelerometer is connected to node 3. Signals from the impact hammer and the accelerometer will be

received by the vibration analyzer for each impact provided one by one and will be compared and analyzed by the software. Curve known as Frequency Response Function (FRF) will be generated by the software that is used to find the natural frequencies of the plate.

C)Analysis of composite plate

FEA involves three stages of activity:

- Preprocessing
- Processing
- Post processing.

In the study, FEA analysis will be is conducted using ANSYS software. To modal the composite plate proper Shell element will be used. The plate is in a fix-free boundary condition. Degrees of freedom are UX, UY, UZ, ROTX, ROTY, ROTZ. We used shell 8node-281 element for lay-up modeling of plate in mechanical APDL.

IV. DATA ANALYSIS

Table I: Natural Frequency with various aspect ratios.

	Frequency in Hz					
	Aspect Ratio 1:1		Aspect Ratio 1:1.5		Aspect Ratio 1:2	
No	Ex	ANSYS	Ex	ANSYS	Ex	ANSYS
1	2	2.117	2	2.42	2.333	2.863
2	6	6.009	6.333	6.417	10.33	9.333
3	14.33	13.72	15.6666	15.875	25.3333	24.095
4	20.33	22.01	28	26.832	29	29.768
5	24.66	24.98	36.6666	35.14	55.3333	58.038
6	42	42.91	49.6666	47.895	59.3333	61.165
7	46	45.22	53.6666	55.422	75.6666	75.31
8	50	51.50	56.3333	56.949	96	102.1

Table II: Natural Frequency with different number of layers

Frequency in Hz					
	10 Layers		15 Layers		20 Layers
No	Ex	ANSYS	Ex	ANSYS	Ex	ANSYS
1	2	1.8001	2.33333	2.1348	2.33333	2.6698
2	5	5.0422	8.66666	8.9161	11.3333	11.161
3	8.66666	7.5992	15.6666	13.419	18.6666	16.884
4	12.6666	12.596	21.6666	22.23	31.6666	31.501
5	17	16.507	25.6666	25.262	42	41.412
6	30	32.103	38	38.21	55.666	56.993
7	49.6666	49.686	51.333	56.478	73.3333	75.099
8	53.3333	56.51	58.3333	60.404	85.6666	86.214

This table clearly shows that the changes in aspect ratio and number of layers change the natural frequency of the plates. These are the 8 mode shapes of the vibration of the plates.

V. RESULTS AND DISCUSSION

Above Data analysis shows that as aspect ratio increases natural frequencies also increases. This results validated by experimental, theoretical and analytical method. In this research, we found a less number of % error between experimental and analytical result. This clearly shows that we did research in a right way.

1) Effect of aspect ratio on natural frequency

To examine the effect of aspect ratio three different types of plates were fabricated, which was made up of 1, 1.5, 2 aspect ratio. The Natural frequency of free vibrations was obtained by experimental, analytical, theoretical method to fix-free boundary condition. The graph of aspect ratio verses frequency plotted below.
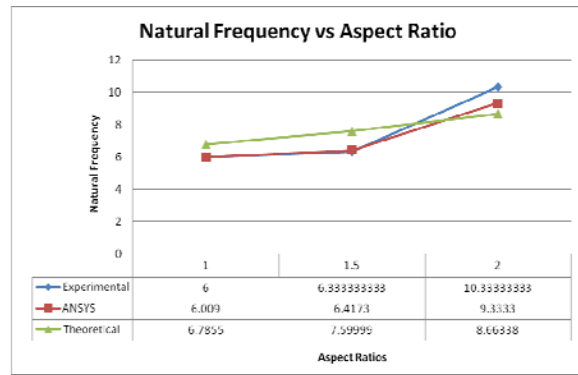
Fig. 3. Effect of fiber orientation on natural frequency.

Above graph clearly shows that as aspect ratio increases the natural frequency also increases as expected. There is a considerable variation in the natural frequency in experimental readings, whereas theoretical calculations shows linearity.
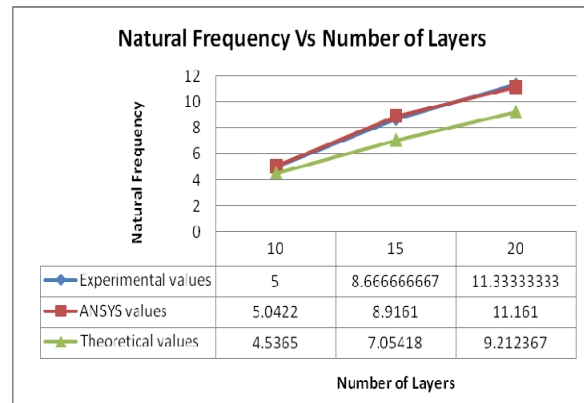
2) Effect of number of layers on natural frequency

Fig. 4. Effect of aspect ratio of natural frequency In order to know the effect of the number of layers on the natural frequency three types of plates were manufactured with different number of layers. The variation of natural frequency with different number of layers shown in fig. 4. The result obtained from free vibration of the plates of both experiment and ANSYS was in good agreement. As observed from fig. 4 numbers of layers have an influence on the dynamic behavior of the laminated plate. As the number of layers increases the natural frequency also increases.

VI. CONCLUSION

In the present study, all experimental, analytical and theoretical study was conducted for woven roving E-glass epoxy composite plate.

Different results were presented to show that the effect of different parameters like aspect ratio and number of layers in fix-free boundary condition. Numerical analysis has been carried out by ANSYS software and the result obtained from ANSYS are giving good agreement with the experimental results. Experimental results and analytical results show some percentage errors because of manufacturing defects, experiment defects, etc., but % errors between them were within range of a good agreement. This experimental method had explored to predict the dynamic behavior of E-glass woven composite plate, in order to design panels or other similar structures used in different applications such as automobile industry, aerospace, civil, marine and other high performance structures.

VII. ACKNOWLEDGEMENT

NOMENCLATURE:

E -Young's modulus of Elasticity
υ -Poisson's ratio
ρ –Density

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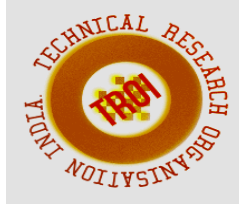
TENSILE TEST AND FEA CORRELATION OF ABS PLASTIC

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Abstract

This paper presents tensile behaviour of ABS polymer. Tensile deformation behaviour of Acrylonitrile Butadine Styrene (ABS) was experimentally investigated, following a practice guideline by ASTM. Tests were performed for various strain rates. Test specimen was prepossessed using CAE software Hypermesh. Results obtained by experimentation were validated using analysis software Abaqus and Ls-Dyna. After ultimate stress, tested Stress – Strain curve had negative slope. During preparation of material card it was a problem. As solver doesn't allow negative slope. Curve was smoothening by establishing a procedure. There was problem with Young's modulus from Stress vs. Strain curve of test results. Some assumptions were made for Young's modulus from test results. It was seen that, specimen thickness contract at higher rate than its width. As strain rate for tensile test increases, its yield stress also increases. Tensile strain rate was maximum in necking region.

Keywords: Tensile test, CAE correlation, Hypermesh, Abaqus, Ls-Dyna.

1. Introduction

Engineering plastics are used in instrument panels, interior trim, fuel tanks and other vehicle applications. Due to their viscoelastic nature, plastics exhibit important rate dependence in their stress–strain responses. The strain rate dependent stress–strain curves of these materials are mandatory input in dynamic finite element (FE) analysis for crashworthiness prediction [9].

The experimental technique to create data at these strain rates is a research topic of practical importance [9]. Modelling and predicting the behaviour of these structures made of polymers require the knowledge of mechanical response of the materials [1].

To obtain valid stress–strain data in a material test, the specimen should be in a state of stress equilibrium, and undergo homogeneous deformation in the gage section. Usually, necking in the polymeric specimen arises at relatively small strain, which results in the inhomogeneous deformation of polymers [1].

2. Material and Specimen

Polymeric material used in this study was Acrylonitrile Butadine Styrene (ABS). Material was specified according to ASTM D638, Type I [14]. It has variation in thickness

from 3.2 mm to 3.8 mm across the length. The specimen has dumbbell shape. The straight gauge section has length of 50mm and width of 13mm [14]. The test dumbbells were injection moulded by the material supplier. The nominal thickness of the specimens was 3.2 mm. Figure 1 shows the geometric dimensions of the test specimen as per ASTM D638 standards [14].
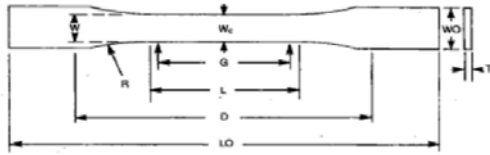

Fig. 1 Geometry and Dimensions of specimen[14].

Table 1. Dimensions for specimen as per ASTM D638 [14].

Dimensions	Type I Specimen	Tolerances
W Width of narrow section	13	±0.5(±0.02)
L – Length of narrow section	57	±0.5(±0.02)
W/O – width overall, min	19	+3.18(±0.125)
LO – Length overall	165	No max
G – Gauge length	50	±0.25(±0.010)
D – Distance between grips	115	+5(+0.2)
R – Radius of fillet	76	±1(±0.04)
T - Thickness	3.2	±0.4

3. Experimentation

ABS dumbbells were tested with UTM machine. Test was conducted according to ASTM D638 test guidelines, which is standard for tensile test of Plastics [14]. Dumbbells were tested with variable strain rate of 10mm/min, and 100mm/min. For each strain rate three specimens were tested. Results obtained are Load (N) and Deflection (mm) for each specimen. From results found calculation performed for Engineering Stress, Engineering Strain, True Stress, and True Strain. Experimentation gives load (N) and Deflection (mm) only. This curve is then converted in to Engg. Stress vs. Engg. Strain and True Stress vs. True Strain curve. Once Young's modulus was finalized, True stress vs. Plastic strain curve was obtained.

A. Calculations

$$Engg. Stress(s) = \frac{Load(N)}{Cross\ Sectional\ Area(Sq. mm)}$$ Equation 1

$$Engg. Strain(e) = \frac{Change\ in\ length}{Original\ Length}$$ Equation 2

$$True\ Strss(\sigma) = Engg. Stress(s)[1 + Engg. Strain(e)]$$ Equation 3

$$True\ Strain(\varepsilon) = \ln[1 + Engg. Strain(e)]$$ Equation 4

$$Plastic\ Starin = True\ Strain - \frac{True\ Stress}{Young's\ Mod.}$$ Equation 5

For calculation of engineering stress cross sectional area of each specimen after break was used. Then calculated Stress for each specimen and averaged it. Curves were plotted with average engineering stress values obtained by calculation.

B. Material Card Preparation

In material card of Hypermesh with profile Abaqus, material type is MATERIAL and card image is ABAQUS_MATERIAL [13].
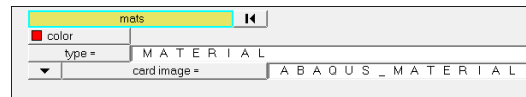

Fig. 2.Material card used in Hypermesh (Abaqus).

In properties of Hypermesh with profile Abaqus, card image used is SOLIDSECTION. Property type is SOLID SECTION [13].
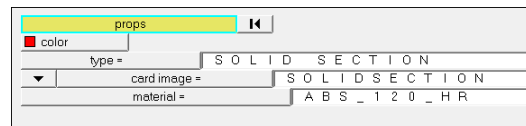

Fig. 3. Property card used in Hypermesh (Abaqus).

In material card of Hypermesh with profile Ls-Dyna Keyword 971, material type is ELASTIC-PLASTIC and card image is MATL24 [12].
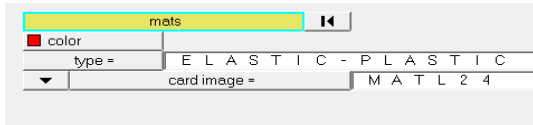
Fig. 4. Material card used in Hypermesh (Ls-Dyna).

In material card of Hypermesh with profile Ls-Dyna Keyword 971, material type is VOLUME and card image is SectSld [12].
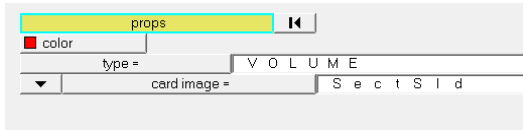

Fig. 5. Property card used in Hypermesh (Ls-Dyna).

For simulation result calculations solver demands plastic strain and True Stress values as input [13, 12]. If given curve have negative slope, its error during performing calculation for Abaqus and Ls-Dyna[12,13]. To exclude this error procedure was established. After ultimate stress where curve starts negative slope those stresses were eliminated performing trial and error to establish smooth curve with positive slope.

Density of ABS is 1.05×10^{-09} tonns/mm³, Poisson's ratio (Nu) is 0.35 for ABS plastic. There was problem with Young's modulus from experimental data. Initially tried young's modules from test results, simulation results obtained with this young's modulus were not as accurate as required. So assumption was made to use value of young's modules for simulation, by performing procedure and made trial and errors on it. A line was drawn at 0.2% strain which is parallel to elastic limit of Stress vs. Strain curve. This procedure gives value of Young's Modulus as 3777.456 MPa.

4. Results

Test results obtained are Load(N) and Deflection(mm). Curves for test results are as:
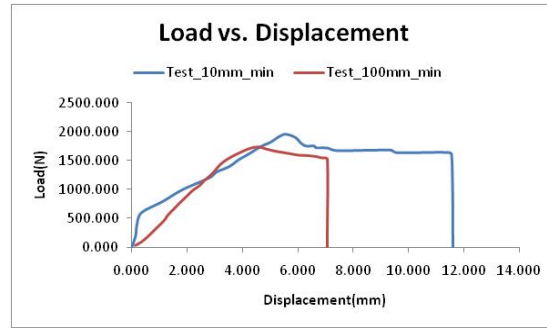

Fig. 6: Load vs. Deflection (Test Results).

From test data of Plastic material, as strain rate is increased ten times Yield value and its elastic limit increases. But total displacement of plastic at break is about half than earlier strain rate.

Data obtained from test were then calculated and converted into Engg. Stress, Engg. Strain, True stress, True strain, and Plastic strain. Curve plotted are with average of all specimen tested for each strain rate.
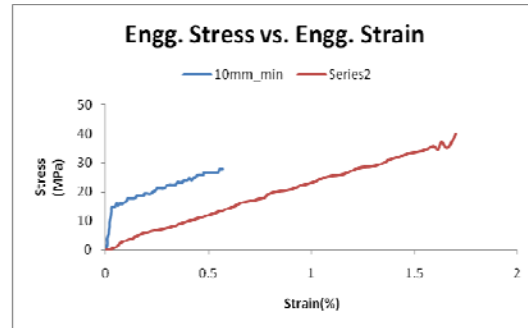

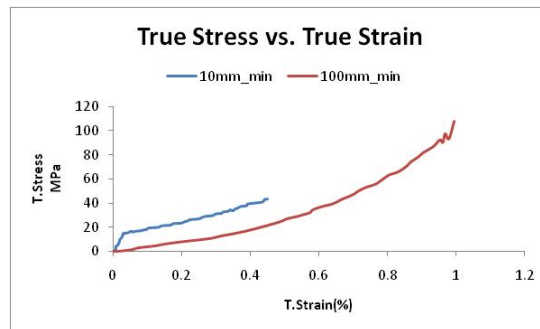Fig. 7: Engg. Stress vs. Engg. Strain.

Fig. 8: True stress vs. True strain.

In the True stress vs. True strain curve, curve shows negative slope after ultimate stress value. As negative slope values are not required by solver for calculations, values of Engg. Stress vs. Engg. Strain and True Stress

vs. True Strain curves are not considered and also not plotted in above graphs (Fig.7 and Fig.8). Abaqus solver needs True stress and Plastic strain values as input. True stress vs. Plastic strain curve also shows negative slope. This was crucial problem during simulation. To resolve this issue, technique was developed. From the observation of curve, it is clear that curve shows negative slope after ultimate stress value. In actual testing, its region where necking formation starts in the test specimen. For the analysis purpose this was very important region of True stress vs. Plastic strain curve.

From the observation of curve, it is clear that curve starts bending after yield stress. Specimen enters in plastic phase from elastic phase. This bending of curve is still considerable, because it shows still positive curve.

Based on trial and error technique, trials were made with region of curve from ultimate stress to breaking point. Trials were made such that curve shows constant slope/positive slope and it will not affect formation of necking region in simulation.
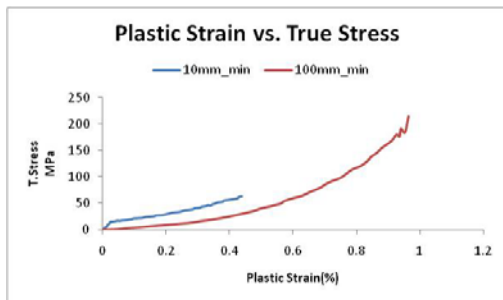

Fig. 9: True Stress vs. Plastic Strain.

Engg. Stress vs. Engg. Strain, True stress vs. True strain and True Stress vs. Plastic Strain curves shows that as strain rate is increasing, its failure value i.e. yield value is also increasing.

A. Correlation of Test and CAE results

Test specimen was first meshed in preprocessor Hypermesh, with profile Abaqus (Standerd3D) and for Ls - dyna with profile keyword971. Specimen was meshed with solid mesh (Hexa elements) with element size 0.5,1

and 1.5mm. After it, counted number of nodes and elements for each type of mesh. From the simulation results noted values of max. stress, strain and displacement for each type of mesh. Results showed that, it is optimum to use 1mm mesh size. Mesh size of 0.5 mm gives better results but it is time consuming for calculation.

One side of dumbbell was constrained with zero degree of freedom and at another side tensile load was applied with only one degree of freedom, allowing specimen to move in only X – direction. Constraints were applied up to 25 mm from both ends as per ASTM D638 standards.

Fig. 10: 1mm element size mesh of dumbbell specimen.

Specimen was simulated in Abaus and Ls-dyna. CAE results in Abaqus shows failure of specimen as actual test specimens.
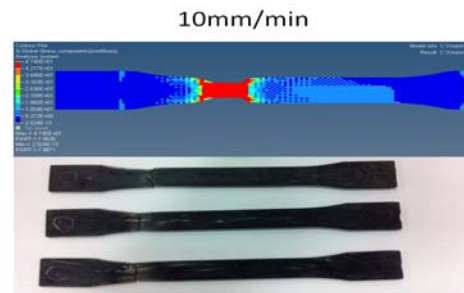

Fig. 11: CAE and Test failure of specimen at 1mm/min strain rate.
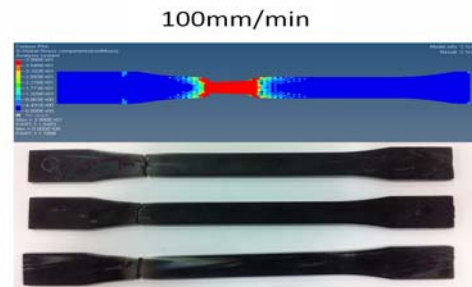

Fig. 12: CAE and Test failure of specimen at 10mm/min strain rate.

From above (Fig.11 and Fig.12) failure figures, it's clearly seen that as test specimen fails, CAE failure is also in the same region of specimen. CAE failure at each strain rate shows that tensile strain rate is maximum in necking region. As in above (Fig.11 and Fig.12) failure correlation is matched, specimens were simulated in Abaqus and Ls-dyna. In both solver failure is analysed and plotted results were also matched.
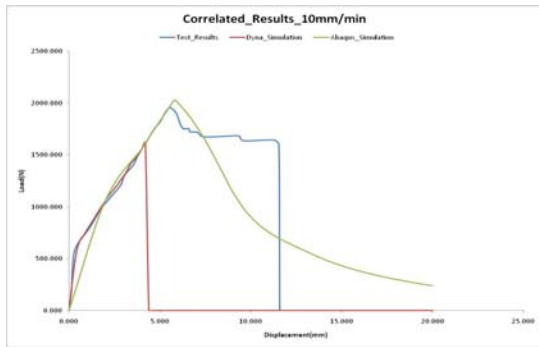

Fig. 13 Correlation of CAE and Test results of specimen at 10mm/min strain rate.
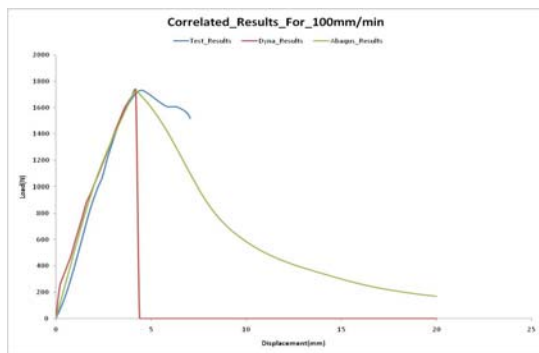

Fig. 14 Correlation of CAE and Test results of specimen at 100mm/min strain rate.

Above graphs (Fig. 13 and Fig.14) shows simulation results obtained in Abaqus and Ls-dyna and Test results obtained are correlated up to Yield point in both cases. From CAE simulation and experimental test it was observed that specimen thickness contract at higher rate than its width.

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DEVELOPMENT OF CATALYTIC CONVERTER FOR EMISSION CONTROL OF STATIONARY DIESEL ENGINE

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Abstract: A catalytic converter is device used to reduce the toxicity of emissions from an internal combustion engine. Also, catalytic converters are most commonly used in motor vehicle exhaust systems. The function of the catalytic convertor is to convert CO, HC and NOx emissions into CO_2, water, N_2 and O_2. In the present work, design specifications of catalytic converter for stationary diesel engine have been presented. According to this design, catalytic converter is developed and then, installed on the single cylinder stationary diesel engine. At the successful completion of present work it is expected that newly designed and developed catalytic converter system will work efficiently to reduce emissions significantly.
Keywords: Catalytic Converter, emissions.

1. Introduction:

Catalytic converters have been widely used on vehicles and have already been proved for many years to be the most effective technical solution to reduce exhaust emissions from gasoline engines. The pollutants have negative effect on air quality, environment and human health that leads in stringent norms of pollutant emission. Numbers of alternative technologies like improvement in engine design, fuel pretreatment, use of alternative fuels, fuel additives, exhaust treatment or better tuning of the combustion process etc. are being considered to reduce the emission levels of the engine. Out of various technologies available for automobile exhaust emission control a catalytic converter is found to best option to control CO, HC and NOx emissions from petrol driven vehicles while diesel particulate filter and oxidation catalysts converter or diesel oxidation catalyst have so far been the most potential option to control particulates emissions from diesel driven vehicle.

There are different catalytic converter systems used. They are as follows.

A. Oxidation Catalytic Converters:

This system ideally converts the oxidising components into H_2O and CO_2. The catalyst operates at excess air settings. The air required for the oxidation process is supplied by lean mixture settings or by secondary air injection. Oxidation catalysts were used for the first time in 1975 on U.S. vehicles. They are no longer used on passenger vehicles today since three-way catalytic converters are far more efficient and will additionally convert NOx emissions. Oxidation catalysts are used to an increasing degree on diesel engines, however, since they are capable of oxidising soluble particulate matter in addition to the above components.[2]

B. Dual-bed Catalytic Converters:

This system includes two catalyst systems mounted in line in the exhaust system. A reduction catalyst is fitted to minimize NOx emissions, and an oxidation catalyst is used to reduce HC and CO emissions. The engine must be operated at air deficiency *(Je< 1)*. This system has therefore certain drawbacks in terms of fuel consumption and *CO2* emissions. Complex mixture formation control systems are not required. Since the engine is operated in the rich Je range, increased ammonia emissions may result. The nitrogen oxide conversion

efficiency is far lower than with three-way catalytic converters.[2]

C. Three-way Catalytic Converters:

A characteristic feature of this system is that is reduces NOx, and HC and CO by the same high degree throughout. To achieve optimum emission control results, however, a complex control system (lambda control) is required. Uncontrolled systems with three-way catalytic converters of the type that was also marketed in Germany only reach conversion efficiencies of approx. 40 to 50%, whereas computer-controlled systems in new condition will reach conversion efficiencies of more than 95%. Three-way closed-loop catalytic converters currently are the most efficient emission control systems available for internal-combustion engines.[2]

D. Denox or Lean-burn Catalytic Converters:

Lean-burn or Denox catalytic converters allow not only CO and HC, but also NOx to be converted in the excess-air range. They are currently in the development stage. NOx conversion efficiencies in excess of 50% have already been demonstrated.[2]

2. Design Specifications of Catalytic Converter:

In this section, specifications of components of catalytic converter system have been presented. This catalytic converter system is designed for Kirloskar stationary diesel engine. The detailed engine specifications are described in experimentation section. From the engine specifications, catalytic converter system is designed. For this design, different parameters like space velocity, volume, shape have been considered. The specifications of designed catalytic converter are shown in following table.

Step 1: Outer Dimensions of Catalytic Converter

Table 1. Dimensions of Catalytic Converter

Catalytic Converter Volume	0.44178 L
Diameter of Catalytic Converter Body	75 mm
Length of Catalytic Converter Body	100 mm

Step 2: Dimensions of Substrate

The dimensions of substrate are selected from volume of catalytic converter. The standard dimensions are shown in following table. Depending on the volume of catalytic converter, 1200/2 cell density diemensions are selected for substrate.

Table 2. Dimensions of Substrate [1]

Parameter	Cell Density			
	400/6.5	600/4	900/2.5	1200/2
Substrate volume, l	0.86	0.67	0.67	0.31
GSA, m^2/l	2.74	3.48	4.37	4.98
OFA, %	75.7	81.4	85.6	83.4
R_f, litres/cm^2	3074	3990	5412	7589
Substrate mass, g	339	202	156	83

These diemensions of substrate 1200/2 cell density are selected because these dimensions gives less emissions as compared to other substrate. The emission results are shown in following table.

Table 3. Emission Reduction [1]

Cell Geometry	Relative HC Emissions	Relative NO_x Emissions
400/6.5	100	100
400/4.5	88	94
600/4.3	65-74	74-93
900/2.5	52-66	59-75
1200/2	41-57	57

3. Material of Catalytic Converter:

In this section, material used for components of catalytic converter have been dicussed. The main components of catalytic converter are –
1. Substrate
2. Catalyst
3. Washcoat

A. Substrate:
The substrate have two functions, first is, it supports the catalyst and second is, takes the catalyst into maximum contact with exhaust gases.
Requirements of Substrate: [1,2]

- Substrate must be covered with the washcoat
- Low thermal inertia and efficient heat transfer
- More surface area per unit volume
- Ability to withstand high operating temperature
- Long durability
- High resistance to thermal shocks

From this requirements, metallic substrate is used in this catalytic converter system and material used as steel because of following reasons.

- Higher mechanical strength
- High thermal conductivity for faster warm-up
- Reduced space requirement and no special mounting is required
- High flow area due to lower cell wall thickness and hence reduced pressure drop
- Higher conversion efficiency[1,2]

B. Catalyst:

The substance which increases rate of reaction without takes part in the reaction is called as catalyst. There are different types of catalysts used for conversion of pollutants. In this, oxides of base metals like copper, chromium, nickel, cobalt etc. and the noble metals like platinum, palladium and rhodium are used. In this investigation, platinum is used as a catalyst because, at high end exhaust temperature base metals oxide becomes deactivate and sintering occurs. Due to this, conversion efficiency of catalytic converter decreases. Another advantage of platinum is good cold start performance.[1]

C. Washcoat:

It is component of catalytic converter which increase the oxygen storage capacity [2]. It increases the surface area of substrate. Alloy coating is done on the washcoat. It consists of Al_2O_3 [2]. Also, titanium dioxide will be used for washcoat as alternative material [3].

4. Manufacturing of Catalytic Converter:

In this section, manufacturing of the components of selected catalytic converter have been discussed. There are three main components of catalytic converter i.e. substrate,

catalyst, washcoat. These components are discussed in above section.

A. Substrate:

An oxidation catalytic converter is a catalyst coated honeycomb-like, channeled metallic substrate, through which exhaust gas passes. The ceramic substrate is constructed by extruding or compressing a ceramic material into a honeycomb structure of desired length and width. Treating the honeycomb substrate with catalyst materials is achieved by drenching the substrate with a slurry containing ceramic and catalytic materials whereby the surface area along the length of every channel is coated and impregnated with catalytic materials. Diesel oxidation catalytic converter substrates are also made from metal foil material which is fan folded and fashioned into a honeycomb substrate with catalyst materials in a similar manner as ceramic substrates. [3]

B. Washcoat:

A washcoat is a carrier for the catalytic materials and is used to separate the materials over a large surface area. The washcoat is a mixture of silica and alumina. The catalytic materials are suspended in the washcoat prior to applying to the core. Washcoat materials are selected to form a rough, irregular surface, which greatly increases the surface area compared to the smooth surface of the uncovered substrate. This in turn maximizes the catalytically active surface available to react with the engine exhaust. The coat must retain its surface area and prevent sintering of the catalytic metal particles even at high temperatures. [1-3]

C. Catalyst:

A catalyst is component of catalytic converter which increases the rate of reaction. In this investigation, platinum is used as catalyst. The coating of catalyst is done on the surface of substrate.

5. Experimental Set-up:

In this section, detail about experimental set up have been discussed. The engine selected for conducting tests is Kirloskar, four-stroke, single-cylinder, water-cooled, naturally aspirated, DI (open chamber), diesel engine. The tests will be performed on experimental set-up shown in Fig. The detail specifications of engine are represented in Table 4. Eddy current dynamometer has been used for loading the engine. The engine will operated at a rated constant speed, 1500 rev∕min.

Table 4. Specifications of Engine

Make and Model	Kirloskar,
No. of Cylinders	One
Orientation	Vertical
Cycle	4 Stroke
Ignition System	Compression Ignition
Bore X Stroke	87.5 mm X 110 mm
Displacement Volume	661 cc
Compression Ration	17.5 : 1
Arrangement of valves	Overhead
Combustion Chamber	Open Chamber (Direct Injection)
Rated Power	5.2 kW (7 HP) @1500 rpm
Cooling Medium	Water cooled

The catalytic converter system is installed with above engine and test will be conducted on this engine such as with catalytic converter system and without catalytic converter system. The photograph of this systems are shown below.

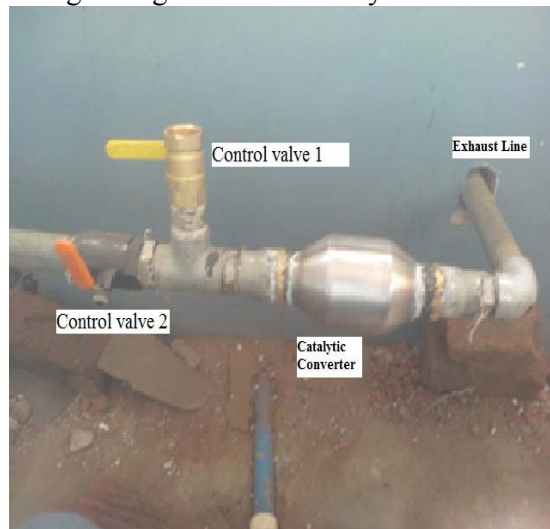Fig. 1 Engine without catalytic converter

Fig.2 Engine with catalytic converter

In above figure, control valve 1, control valve 2, catalytic converter and exhaust line are shown. The control valve 1 is used for injection of diesel exhaust fluid for reduction of NOx emission. The diesel exhaust fluid is a solution of urea and water. In this investigation, catalytic converter is connected in exhaust line of engine with the help of brazing.

6. Conclusion:

From study of designed catalytic converter, suitable material for components of catalytic converter is selected. The parameters required for design of catalytic converter are identified. The designed catalytic converter is successfully manufactured and installed with engine. The

installed catalytic converter will reduce emissions significantly.

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DRY SLIDING WEAR BEHAVIOR OF AS CAST AL-30MG2SI-4FE ALLOY

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Abstract— In present work, dry sliding wear behavior was investigated on a pin on disc wear testing machine at constant sliding velocity 1-4m/s and normal load 10-50N. As the sliding velocity increases, the coefficient of friction decreases. Tribo surfaces were investigated by optical microscopy and reveals that the majority of wear is due two body abrasive mechanism. Wear behavior of material is a common phenomenon when two surfaces are into contact, the nature of the wear depends upon large number of variables like temperature, sliding velocity, nature of surface contacts, type of materials, applied loads and many more. In the present work an attempt is carried out to minimize the wear rate by using various compositions. Further, it was observed that at lower speeds and lower loads the wear rate accordingly decreases and increases by an increase in loading. At constant load of 10N the rough surface nature of contact was observed and resulted in more wear rate. It was also observed as the sliding velocity increases to 4m/s the wear rate decreases by 17% and due to surface contact time decreases.

Keywords—Al-30Mg$_2$Si-4Fealloy,Dry sliding, Microstructure, Wear Rate.

I. INTRODUCTION

In the recent years, the demand of automobile industries for design of newer light weight (high strength to weight ratio) material has been greatly increasing with high strength, excellent wear and corrosion resistance [1]. Al-Si alloy has created a lot of interest and has become a prime material for both automobile and aircraft components [2]-[5]. With the increase in the silicon content, the alloy gives excellent hardness, low density and also improves the wear resistance [3]-[4]. Research has emphasized that by adding the transition metals like Fe and Cu to Al-Si alloys showed a improvement in wear resistance. Also adding of iron in Al-Si alloys decreases mechanical and tribological properties due to the formation of long and brittle needle like β-Al$_5$FeSi intermetallics [5]-[6]. The dry sliding wear behavior of Al-Si alloys depends on distribution of Si particles in the Al matrix. In order to improve mechanical properties of this alloy, Mg and Fe are added as alloying elements. Cu and Fe are also the alloying elements considered to be more promising for producing Al-Si alloy with improved properties [1]-[2]. Amongst the most aluminium casting alloy, Aluminium-silicon alloys are most common alloys having an attractive characteristics such as high strength to weight ratio, good mechanical and thermal conductivity and corrosion resistance. Aluminium-silicon was found to have wide variety of application in cylinder blocks and heads, piston and engine parts, rocker arms, impellers etc [4]. Recently it has been shown that addition of Fe to this alloy showed Increase in hardness and also

improved the wear resistance but with the increase in percentage of Fe content further increased the hardness but decreased the wear resistance of the alloy. A large reduction in density is thought to be great boon for automotive industries [4]-[5]. These leads to the formation of Mg_2Si an intermetallic compound which results in the improvement of mechanical properties. Al-Si alloys, the size and morphology of primary and eutectic silicon phases have vital importance in terms of mechanical properties. Al-Si-Fe alloys have been studied extensively to ensure reasonable mechanical or tribological properties [7]. For adhesive and abrasive wear processes it was shown that the material removed is directly proportional to sliding distance and the normal load and is inversely proportional to hardness[8]-[9]. Wear of a material is controlled by the material characteristics as well as operating parameters such as applied pressure, sliding speed, environment and type of sliding interaction[10]-[12].

II. EXPERIMENTAL PROCEDURE

2.1. Material and characterization

The alloy used in the present investigation is light weight heat treatable. Commercially available alloy was purchased from FENFE Metallurgical, Bangalore, India. Table 1 summarizes the chemical compositions of the selected alloy. The material was cut into these specimens with dimensions of 30mm length and 10mm diameter. The dimensions are maintained according to ASTM E8 standards. The alloy used in the present work is Al-30Mg2Si-4Fe. The microstructure characterization of alloy was carried out by optical microscope.

Table 1: Chemical composition (wt %) of Al-30Mg2Si-4Fe alloy

Alloy %	%Mg	%Si	%Fe	%Cu	%Al
Al-30Mg2Si-4Fe	16.89	12.71	3.74	0.003	Bal

2.2. Wear testing

The dry sliding wear test of as cast alloy was carried out at room temperature on pin on disc wear testing machine (Model: TR-20, DUCOM).

The specimens were of 30mm length and 10mm diameter with machining the surface of the specimens. The wear testing was conducted under various normal loads of 10, 30, 40 and 50N at various sliding velocities of 1, 2, 3 and 4m/s. All the specimens were weighed after each of the tests been conducted at various loads and at various sliding velocities. The wear rates of the alloy are calculated by measuring the difference in weight of the specimens measured before and after the tests. Further frictional force, wear rate, loss of material by volume, coefficient of friction etc were measured. The study of wear debris and worn out surfaces were done by SEM images. The following Fig. shows the pin on disc wear testing machine on which wear test of as cast Al-30Mg2Si-4Fe alloy were conducted.

Fig. shows photograph of Pin-on-disc wear testing machine (TR-20)

III. RESULTS AND DISCUSSION

The optical micrographs of Al-30Mg2Si-4Fe alloy as cast samples before and after wear are shown in Fig. 1 (a-d)

As cast Al-Mg2Si-4Fe alloy

The microphotograph of optical microscopy shows Mg and Si are distributed uniformly throughout the surface. Si repressnts needle like structure and Mg appears like platelets and the black appears to be

Fe. The Aluminium bieng the soft matrix and Mg and Si are hard particles which are distributed uniformly and resist the wear. This also reduces the heat generation and hence these alloy does not get over heated.The needle like structures reduces the contact surface area of bulk matrix and softens the alloy hence aluminium does not deform. Mg particulates are hard particles and thus increases the volume surface area,thus better the distribution of reinforced particles decreases the volume wear rate.
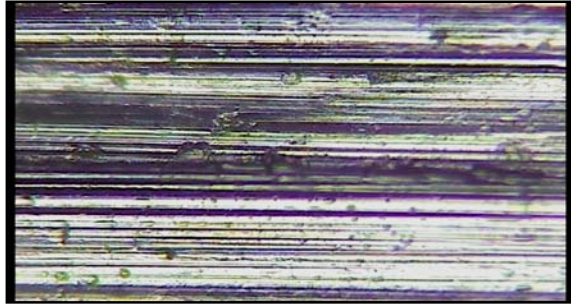
Fig.1a Optical microscopy image of 1m/s at sliding velocity of 10N
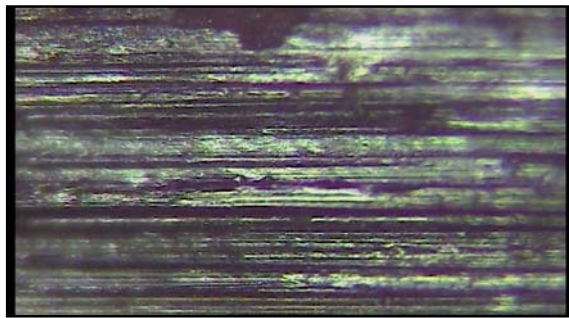
Fig.1b Optical microscopy image of 2m/s at sliding velocity of 10N
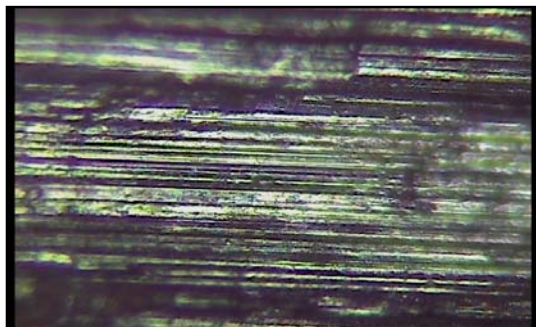
Fig.1c Optical microscopy image of 3m/s at sliding velocity of 10N

Fig.1d Optical microscopy image of 4m/s at sliding velocity of 10N
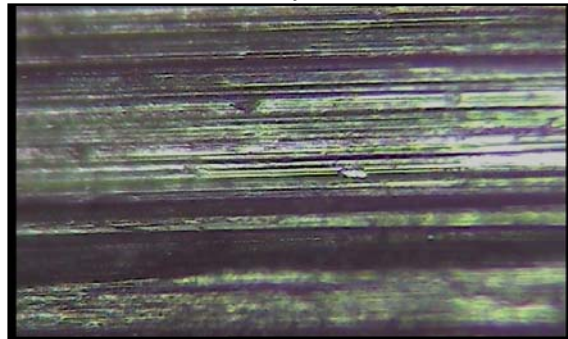
The Fig.1a shows worn out surfaces at siding velocity of 1m/s at constant load of 10N. The wear of an alloy is demonstrated by the microphotograph which shows the 2 body abrasive wear mechanism. The plough lines indicate a continuous contours and Al matrix is deformed due to large ductility, however due to Mg, Si hard particles dispersions the wear rate is reduced and small contours indicate that the alloy is harder and act as a resistance to abrasion decreasing the wear rate. Figs. 2(a-d) show the wear rate (volume loss of the material) and (coefficient of friction) against varying load and speed of Al-30Mg$_2$Si-4Fe alloy.
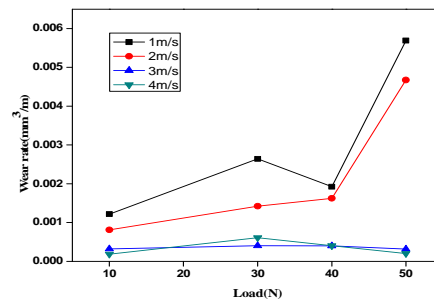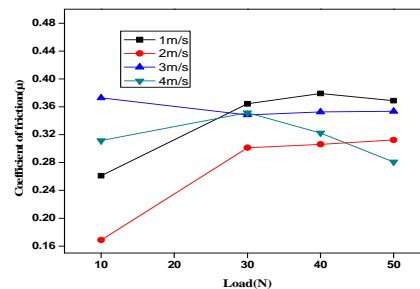
Fig 2a Wear rate v/s Load
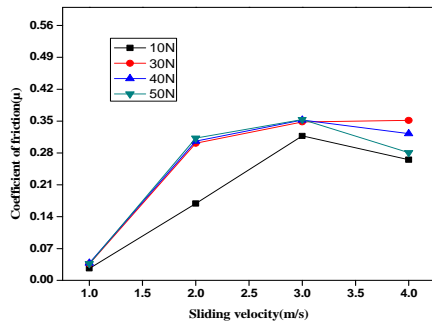
Fig.2b Coefficient of friction v/s Load

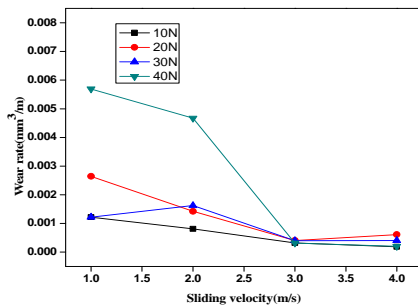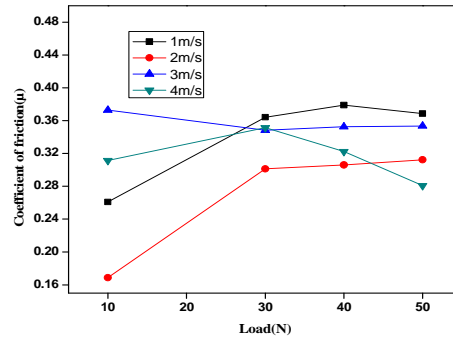Fig.2c Wear rate v/s Sliding velocity

Fig, 2d Coefficient of friction v/s Sliding velocity

Fig. 2a shows volume loss of material at various loads by keeping sliding velocity constant. It is observed that wear rate increases as load increases but decreases as the sliding velocity decreases. Fig. 2b shows coefficient of friction at various loads by keeping sliding velocity constant. It is clear from the graph that the coefficient of friction increases with an increase in the load up to 30N and further a sudden decrease in the slope is observed from 30 to 50N. This sudden decrease occurs with a increases in the sliding velocity. Fig. 2c shows wear rate against sliding velocity with a constant load. In this graph the wear rate decreases as the sliding velocity increases up to 3m/s and further shows linearity from 3 to 4m/s. This might be due to the transition from abrasive to abrasion wear mechanism and finally Fig. 2d shows a graph coefficient of friction at various sliding velocity with constant load. This graph reveals that coefficient of friction increases at initial point of sliding velocity 2m/s and then gradually decreases at 4m/s but decreases with the increase in the constant load.

IV. CONCLUSION

1. An alloy with many elements will exhibit higher wear resistance then just one element.
2. At 40N wear rate gradually decreased and then sudden increase at 50N with the different constant sliding velocity.
3. Whereas coefficient of friction decreases with increase in load.
4. At varying speed there is increase in wear rate as speed increases with different constant load.
5. Coefficient of friction decreases with increase in speed, as contact surface time is less.

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