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Technical Research Organisation India (TROI) is pleased to organize the International Conference On Advance Engineering and Technology (ICAET-2014).

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Editorial

The conference is designed to stimulate the young minds including Research Scholars, Academicians, and Practitioners to contribute their ideas, thoughts and nobility in these two integrated disciplines. Even a fraction of active participation deeply influences the magnanimity of this international event. I must acknowledge your response to this conference. I ought to convey that this conference is only a little step towards knowledge, network and relationship.

The conference is first of its kind and gets granted with lot of blessings. I wish all success to the paper presenters.

I congratulate the participants for getting selected at this conference. I extend heart full thanks to members of faculty from different institutions, research scholars, delegates, TROI Family members, members of the technical and organizing committee. Above all I note the salutation towards the almighty.

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DRAINAGE ON ROADS

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ABSTRACT:

It has been seen many times that water in pavements is one of the major causes of premature pavement failure. Water may enter the pavement due to various reasons which may be stagnation of water on the surface or faulty construction of the roads leading to seepage of water into the pavement and thus causing damage to the same. Water in the pavement system can lead to moisture damage, modulus reduction and loss of strength. In order to prevent such damages to the pavement, it is essential to provide proper drainage to the roads. The presence of water in a highway layer reduces the bearing capacity of the road, and in doing so it also reduces the structure's lifetime. Highway drainage is used to clear surface water from the highway. . Roads need to be well drained to stop flooding, even surface water can cause problems with ice in the winter. Water left standing on roads can also cause maintenance problems, as it can soften the ground under a road making the road surface break up.

1. INTRODUCTION:

Highway drainage is the process of removing and controlling excess surface and sub-surface water within the right way. This includes interception and diversion of water from the road surface and sub-grade. The installation of suitable surface and sub-surface drainage system is an essential part of highway design and construction.

During rain, part of the rain water flows on surface and part of it percolates through the soil mass as gravitational water until it reaches the ground water below the water table. Removal and diversion of surface water from the roadway and adjoining land is termed as surface drainage, while the removal of excess soil-water from the sub-grade is termed as sub-surface water.

2. NECESSITY OF HIGHWAY DRAINAGE

Highway drainage is important from various view points:

➢ Excess moisture in soil sub-grade causes instability under the road surface. The pavement may fail due to sub-grade failure. In some clayey soil variation in moisture content causes considerable variation in volume of sub-grade. This sometimes contributes to pavement failure.

➢ The waves and corrugations formed in case of flexible pavements also play an important role in pavement failure.

➢ Sustained contact of water with bituminous pavements causes failure due stripping bitumen from the aggregates like loosening of some of the bituminous pavement layer and formation of pot holes.

➢ The prime cause of failures in rigid pavements by mud pumping is due to the presence of water in fine sub-grade soil.

➢ Excess water on shoulders and pavement edge causes considerable damage.

➢ Excess moisture causes increase in weight and thus increase in stress and simultaneous reduction in strength in soil mass. This is one of the main reasons of failure of earth slope and embankment foundations.

➢ In place where freezing temperatures are prevalent in winter, the presence of water in sub-grade and a continuous supply of water from the ground water can cause considerable damage to the pavement due to in frost action.

➢ Erosion of soil from top of un-surface roads and slopes of embankment, cut and hill side is also due to surface water.

➢ Failure due to hydraulic pressure and failure due to binder stripping can be avoided with the help of proper drainage on roads.

3. ROAD DRAINAGE

Well designed and well maintained road drainage is important in order to:

• Minimize the environmental impact of road runoff on the receiving water environment.

• Ensure the speedy removal of surface water to enhance safety and minimize disruption to road users.

• Maximize the longevity of the road surface and associated infrastructures.

There are many different types of drainage systems with different design features and attributes that can be used to manage flows and treat water quality. Drainage which is needed on the Highways Agency network depends not just on any flood risks and pollution risks identified but the characteristics of the natural water catchment area in which the network is based. The size, shape, gradient and geology of a catchment area are all factors which can influence the type of drainage methods used.

4. SURFACE DRAINAGE

The surface water is to be collected and then disposed off. The water on the surface is first collected in longitudinal drains, generally in side drains and then the water is disposed off at the nearest stream, valley or water course. For the preparation of surface drainage, we should keep in mind various things like

COLLECTION OF SURFACE WATER

Seeing the amount of rainfall and slope a suitable camber is to be provided for collection of surface

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water. The shoulders of rural roads are constructed with suitable cross slopes so that the water is drained across the shoulders to the side drains. These side drains of rural roads are generally Open (kutcha) drains of trapezoidal shape, cut to suitable cross-section and longitudinal slopes. These sides are provided parallel to the road alignment and hence these are also known as longitudinal drains. In embankments the longitudinal drains are provided on one or both sides beyond the toe; in cutting, drains are installed on either side of the formation.

In urban roads because of the limitation of land width and also due to the presence of footpath, diving island and other road facilities, it is necessary to provide underground longitudinal drains. Water drained from the pavement surface can be carried forward in the longitudinal direction between the kerb and the pavement for short distances which may be collected in catch pits at suitable intervals and lead through underground pipes.

Drainage of surface water is all the more important in hill roads. In hill roads disposal of water is also very important. Certain maintenance problems may arise due to faulty hill road construction.

5. CROSS DRAINAGE

For streams crossing the runways, drainage needs to be provided. Also often the water from the side drain is taken across by these cross drains in order to divert the water away from the road, to a water course or valley in the form of culverts or bridges. When a small stream crosses a road with linear water way less than amount six meter, the cross drainage structure provided is called culvert; for higher value of linear waterway, the structure is called bridge.

6. SUB-SURFACE DRAIN

Change in moisture content of sub-grade are caused by fluctuations in ground water table seepage flow, percolation of rain water and movement of capillary water and even water vapour. Although sub-surface drainage helps in removal of gravitational water, it is designed to keep minimum moisture in sub-grade.

LOWERING OF WATER TABLE

The highest level of water table should be fairly below the level of sub grade, in order that the sub grade and pavements layers are not subjected to excessive moisture. From practical considerations it is suggested that the water table should be kept at least 1.0 to 1.2 meter below the sub grade. In place where water table is high (almost at ground level at times) the best remedy is to take the road formation on embankment of height not less than 1.0 to 1.2 meter. When the formation is to be at or below the general ground level, it would be necessary to lower the water table.

If the soil is relatively permeable, it may be possible to lower the high water table merely construction of longitudinal drainage trenches with drain pipe and filter sand. If the soil is relatively less permeable, the lowering of ground water level may not be adequate at the center of the pavement or in between the two longitudinal drainage trenches. Hence in addition, transverse drainage may have to provide in order to

effectively drain off the water and thus lower the water table up to the level of transverse drains.

7. PREVENTIVE MEASURES

• CONTROL OF SEEPAGE FLOW

When the general ground and impervious strata below are slopping, seepage flow is likely to exist. If the seepage zone is at depth less than 0.6 to 0.9 meter from the sub grade level, longitudinal pipe drain in trench filled with filler material and clay seal may be constructed to intercept the seepage flow.

• CONTROL OF CAPILLARY RISE

If the water reaches the sub grade due to capillary rise is likely to be detrimental, it is possible to solve the problem by arresting the capillary rise instead of lowering the water table. The capillary rise may be checked either by capillary cut-off of any one of the following two types:-

a) A layer of granular material of suitable thickness is provided during the construction of embankment, between the sub grade and the highest level of sub surface water table.

The thickness of the granular capillary cut-off layer should be sufficiently higher than the anticipated capillary rise with in the granular layer so that the capillary water cannot rise above the cutoff layer.

b) Another method of providing capillary cut-off is by inserting an impermeable or

Bituminous layer in the place of granular blanket.

8. CONCLUSION

Seeing the above properties of drainage and keeping in view the necessity of drainage at surface as well as sub-surface level,

drainage plays an important role in highway engineering. As drainage helps in avoiding various types of failures as may be caused by stagnant water on the road surface or its seepage beneath the pavement, it is important to provide drainage facility while construction of roads. Thus to increase the life of the road and to reduce the maintenance cost drainage of roads must be properly provided. Considering the above factors, this paper has been attempted in lieu of highway engineering.

REFERENCES:

1. https://mailattachment.googleusercontent.com
2. https://mailattachment.googleusercontent.com
3. http://www.highwaysmaintenance.com/drainage.htm
4. *http://www.wq.uiuc.edu/dg/surface.htm*

IMPORTANCE OF ROADSIDE VEGETATION

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ABSTRACT

Roads are the integral part of transportation system. It plays a significant role in achieving national development and with the help of road side vegetation and by selecting right species of plant at right area we can reduce the maintenance needs and cost of road, provides safety for vehicles, improves the overall driving experience of roads, reduce soil erosion.

Enhance the drainage aspect of roads as vegetation increase the water infiltration capacity of soil, improves the shear strength of embankments by controlling the moisture content and increase the life of shoulder. Beside all these factors vegetation also cover the environmental aspect such as control noise pollution, air pollution and maintains the ecological balance and aesthetic view.

1. INTRODUCTION

As with growing time government of every country wants the best & economic technique should be adopted in each part of the country & an attempt is made by the engineers to find the alternatives of each technique. The Roadside vegetation or bio engineering is a technique through which the life of road can be increased by controlling the moisture content of soil, by improving shear strength of soil, by improving infiltration capacity of soil & by controlling soil erosion. Through this technique we can also reduce the cost of construction, maintenance cost of roads.

The road side vegetation technique or bio engineering technique requires assessment of existing road condition determination of type of roadside environment desired according to increased public demand and customer expectations. There are various factors on which vegetation techniques depend:

 Soil conditions;   Traffic Composition;

Location of road;   Topography; Adjacent

Land Use;   The Priority of Road;   Aesthetic appearance

It is a rapidly growing field subject to innovations & changing design specifications. Due to increased environmental awareness this technique is beneficial than traditional approaches.

2. BENEFITS OF VEGETATION

2.1 ECONOMIC ASPECTS

- Improved Road side conditions enhance the visitor visit.
- Reduce cost of construction activities due to less requirement of improved technology.
- Also improves life of pavement. (This technique can be used in soil stabilization situations)
- It also reduces maintenance cost and needs.
- It improves water infiltration capacity of soil & reduces run off.
- The roots, stems & associated woods that we obtained from cutting are used to build the structures.
- Traditional method of controlling stream flow & wave induced erosion on embankment have relied on structural practice like retaining wall & sheet piles which are expensive, ineffective whereas Bio engineering technique as one of best economic alternative approach.

2.2 ENVIRONMENTAL ASPECTS

- It improves air quality by absorbing carbon monoxide, and carbon dioxide.
- It also stabilizes the ground surface to prevent soil erosion as with time the strength of root system increases which increase the soil stability and the soil is less prone to soil erosion.
- Provides habitats for wildlife.
- Control weeds on roadside conditions.
- Increased biodiversity (variation of species)

2.3 SAFETY ASPECTS

- Vegetation proves an effective tool for slope protection in road projects.
- It minimizes effect of rain, snow and ice formation.
- It also minimizes hazardous conditions for maintenance staff.
- It reduces the slippery on the roads and provides safety for vehicles.

3. BENEFITS OF VEGETATION ON EMBANKMENTS

In Embankment design slope stability is the major consideration or element on which design of embankments depends and there is complex relationship between vegetation and slope stability. Vegetation enhance slope stability in following ways:-

By Removing water from soil

(i) Due to shading of trees, the soil becomes dry which increases the infiltration capacity of the soil and allows deep penetration of the rain water.

(ii) Due to capillary action of plants the r is drawn up from the roots or soil to the leaves which is then removed through process of transpiration it also by controlling moisture content of soil.

Mechanical Reinforcement

i. Roots increase the shear strength of the soil by binding the particles along the potential failure plant.

ii. Due to root elongation across slip plane there is development of root tensile force which is transferred to soil.

4. EFFECT OF VEGETATION ON SHOULDER

A shoulder is a portion of roadway that is continuous with the travelled way and is provided for lateral support of base and surface course. Due to lack of funds most common types of shoulder prevail in India are earthen shoulders that are compacted in different layers. Due to earthen shoulders maintenance requirement is an essential component and vegetation plays a vital role in maintaining shoulders during rainy season as it prevent the rain cuts, reduce slipperiness of the shoulder. Improves the water Infiltration capacity of the shoulder and also avoid soil erosion during rainy season by firmly biding the soil particles. Vegetation is also the one of way of keeping the earthen shoulder in proper shape of profile. With the help of vegetation dust nuisance is also minimized and load carrying capacity of shoulder is also increased.

5. IMPORTANCE OF VEGETATION ON HILL ROADS

As hill ranges are very young due to which a minor disturbances can cause slips, subsidence and Land-slides. Landslides are basic problem on all hill roads. There are many factors which contribute the land slide whereas deforestation, grazing of animals is also a major contributing factor. As trees or vegetation on roadside not only increase shear strength along the failure plane but also improves the load carrying capacity of soil along the failure plane, provides lateral support by preventing soil erosion. As a preventive measure to avoid landslides afforestation & fencing should be done so that grazing of animals should be stopped.

6. AESTHETIC ASPECT OF VEGETATION

- Roadside vegetation protects from unsightly views such as slums, Junk Yards, Storage depots etc.
- Trees provide shade, colour if they are of flowering variety and also yields fruits.

7. ENVIRONMENTAL ASPECT OF VEGETATION

Noise Pollution: Noise is an unwanted sound on the road &it is mainly caused by breaks, horn, and engine of vehicles. So for highway engineering it is also a better opportunity to control noise pollution by just planting the trees and shrubs on the roadside.

Air Pollution: As lot of poisonous fumes and smell are caused by the engines of vehicles which are hazardous to environment and driver. All types of pollutant like lead particles, oxides of nitrogen, Carbon monoxide, Oxides of nitrogen can be easily controlled by the roadside vegetation.

8. LIMITATIONS OF VEGETATION

- Vegetation doesn't stabilize instable slopes as due to higher planting difficulties and a higher erosion hazard produce by greater runoff velocity.

- Improper drainage and poor consolidation of roads are less stabilized by vegetation.
- The availability of easily adapted plants may be limited.
- Labour needs are intensive & skilled experience labour may not be available. So pre-requisite training is required.
- The planting season of plant or vegetation may be limited.
- If trees are planted at top of slope extra 10% factor of safety should be required as tree of 30-50m height generally applies loading of 150km/m^2.

9. SPECIES SELECTION

It should be beneficial to select native species instead of non-native species as these can easily compete with the prevailing climatic conditions and one should try to select those species of vegetation that can roughly match with the environmental conditions of road and special attention should be given in following cases:-

- Select those species with that are comfortable with soil movement at project sites.
- The deep and widespread root system should be adopted where deep earth movements are there. E.g.: Popular, Eucalypts Acacia.
- Special attention should be given in shady regions as most of plants material will grow poorly and their life is also short.

10. CONCLUSION

Although roadside vegetation has certain limitations like limited plantation season of trees but keeping in view all the above benefits of roadside vegetation, considering its economic, environmental, safety aspect etc. ; it should be given due importance.

Since, roadside vegetation has varied benefits on hilly roads, embankments, to improve soil strength, improving infiltration capacity of soil, reduction in soil erosion. So considering the benefits of roadside vegetation, this paper has been attempted to promote roadside vegetation as an important aspect in Highway Engineering.

REFERENCES:

1. Pandey DK & Rao Nilanjana, "Bio-Engineering Techniques for slope protection in road projects", Journal of Indian Highways, April 2004.
2. Kadyali LR & Lal N.B., "Principle and practice of highway engineering, sixth edition, 2013".
3. http://en.wikipedia.org/wiki/Vegetation_and_slope_stability
4. http://www.lrrb.org/media/reports/200820.pdf

AN INVESTIGATION OF STRENGTH CHARACTERISTICS OF CONCRETE CONTAINING RECYCLED AGGREGATES OF MARBLE AND GRANITE WASTE.

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Abstract— **The results obtained from the present investigation on strength characteristics of concrete containing natural aggregates and natural aggregates with partial replacement by marble and granite waste aggregates in different percentages have been presented. In the series of test conducted when natural aggregates were replaced by marble waste and granite waste aggregates used in equal proportions with replacement of natural aggregates by 20% (10% marble +10% granite) , 30% (15% marble +15% granite),40% (20% marble +20% granite) were cast. The compressive strength of specimens were tested for mixes containing marble and granite waste as recycled aggregates increased for replacement 20% and 30%. However for the 40% replacement of marble and granite waste aggregate with natural aggregate a marginal decrease in compressive strength is recorded. Therefore it can be concluded that the production of concrete of normal strength is feasible and viable by replacing the natural aggregates by the waste marble and granite aggregates without compromising the strength characteristics.**

Index Terms—**Specific Gravity, water Absorption , Fineness Modulus and Compressive Strength.**

I. INTRODUCTION

Recycling is the act of processing the used material for use in creating new product. Stone waste i.e. Marble and Granite waste has been commonly used as building materials. Today industry's disposal of stone waste is one of the environmental problems around the world .Stones are cut into smaller blocks in order to give them the desired shape and size. During the process of cutting, the original stone mass is lost by 30%. The waste is dumped in nearby pits and vacant spaces. This leads to serious environmental pollution an occupation of vast area of land. So it poses a severe threat on the environment, eco-system and the health of the people. The Quarrying and Trimming waste also poses a serious environmental damages.

So it is necessary to use this stone waste in construction industry. Recycled aggregate of Marble and Granite waste are comprised of crushed, graded inorganic particles processed from the materials that have been considered as a waste material. In the present study an effort has been made to explore the possibility of using these materials as part replacement of natural aggregates for making concrete.

Terzi and Karasahin (2003) investigated the use of marble dust in asphalt mixtures as a filler material for optimum filler/bitumen and filler ratio. They have concluded that marble wastes in the dust form could be used in such cases.

Abkulut and Cahit (2007) studied the use of marble quarry waste in asphalt pavements with bitumen. They reported that waste materials can potentially be used as aggregates in light to medium trafficked asphalt pavement binder layers.

Binici etal. (2008) studied durability of concrete

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containing granite and marble as coarse aggregates. The result indicated that marble, granite and ground blast furnace slag replacement provide a good durable concrete.

Wattanasiriwech et al. (2009) investigated the use of waste mud from ceramic tile production in paving blocks and determined compressive strengths of these blocks. They observed that the blocks containing cement 20 weight% gave satisfactory strength values.

Pereira et al. (2009) performed an experimental study using a number of coarse aggregates from different geological sources including granite, basalt, limestone and marble. They produced concretes in specific mix proportions and laboratory controlled conditions. They explored that concrete durability properties were not affected by aggregates mineralogy, but in turn were significantly affected by the aggregate size and its water content.

Padmini et al. (2009) investigated the properties of recycled aggregates from parent concrete (PC) of three strengths, each of them made with three maximum sizes of aggregates. They produced recycled aggregate concrete (RAC) using these recycled aggregates. They found that RAC required relatively lower water-cement ratio as compared to PC to achieve a particular compressive strength. They also determined that the difference in strength between PC and RAC increased with strength of concrete.

Martínez-Barrera and Brostow (2010) studied effects of gamma irradiation and the marble particle size on compressive properties and the dynamic elastic modulus of polymer concretes. One of the conclusions was that both compressive properties and the dynamic elastic modulus values depend on the combination of the marble particle sizes and the applied radiation dose. Higher numbers of dispersed particles per unit volume provide more resistance to crack propagation. Medium size marble particles provide better compression modulus.

II EXPERIMENTAL PROGRAMME

The test programme consisted of the testing of the constituent materials i.e. cement, fine aggregate, coarse aggregate as per relevant Indian Standard Codes of Practice and testing of specimens containing Natural aggregates and with recycled aggregates of marble for compression and split tensile strength. The physical properties of cement used in the present study are given in Table 1. The physical properties of fine and coarse natural and granite aggregates used in investigation are presented in Tables 2, 3, 4 and 5.

Table 1: Physical Properties of Cement

Sr. No.	Property	Experimental value
1	Consistency of Cement	30%
2	Specific Gravity	3.14
3	Initial Setting Time	92 minutes
4	Final Setting Time	298 minutes
5	Comp. Strength i) (N/mm^2) ii) 3 days iii) 7days 28 days	24.67 35.04 47.28
6	Fineness (Dry Sieving)	2.5 %

Table 2: Physical Properties of Fine Aggregates

Characteristics	Results Obtained
Grading	Grading Zone II (IS: 383-1970)
Fineness Modulus	2.55
Specific Gravity	2.62
Water Absorption (%)	0.48%
Free Moisture Content (%)	Nil

Table 3: Physical Properties of Coarse Natural Aggregates

Characteristics	Results Obtained
Fineness Modulus	6.6
Specific Gravity	2.66
Water Absorption (%)	0.50%
Moisture Content (%)	Nil

Table 4: Physical Properties of Coarse Marble Aggregates

Characteristics	Results Obtained
Fineness Modulus	6.51
Specific Gravity	2.68
Water Absorption (%)	0.32
Moisture Content (%)	Nil

Table 5: Physical Properties of Coarse Granite Aggregates

Characteristics	Results Obtained
Fineness Modulus	6.51
Specific Gravity	2.70
Water Absorption (%)	0.49
Moisture Content (%)	Nil

Sieve analysis of fine aggregates, coarse natural, marble and granite waste aggregates is carried out and the results are presented in Tables 6, 7, 8 and 9. The details of mixes
with and without marble and granite waste aggregates are given in Table 10.

Table 6: Sieve Analysis of Fine Aggregates

IS Sieve Designation	Wt. Retained on Sieve (gm)	Cumulative Weight Retained (gm)	Cumulative Percentage Weight Retained (gm)	%age Passing
10mm	0.00	0.00	0.00	100.00
4.75 mm	15.10	15.1	1.51	98.49
2.36 mm	25.20	40.30	4.03	95.97
1.18 mm	250.10	290.40	29.04	70.96
600 μ	160.00	450.40	45.04	54.96
300 μ	320.10	770.50	77.05	22.95
150 μ	217.10	987.60	98.76	1.24
Pan	12.40	1000	-	-

Table 7: Fineness Modulus of Proportioned Coarse Aggregates

I S Sieve Designation	Wt. Retained on Sieve (10 mm Agg) (gm)	Wt. Retained on Sieve (20mm Agg) (gm)	Average Weight Retained (gm)	Cumulative Wt. Retained (gm)	Cumulative %age Wt Retained (gm)	%age Passing
80mm	0.00	0.00	0.00	0.00	0.00	100.00
40 mm	0.00	0.00	0.00	0.00	0.00	100.00
20 mm	0.00	335	167.5	167.5	3.35	96.65
10 mm	1225	4565	2895	3062.5	61.25	38.75

4.75 mm	3625	90	1857.5	4920	98.40	1.6
Pan	-	-	-	-	-	-

Table 8: Fineness Modulus of Proportioned Coarse Marble Aggregates

I S Sieve Designation	Wt. Retained on Sieve (10mm Agg) (gm)	Wt. Retained on Sieve (20mm Agg) (gm)	Average Weight Retained (gm)	Cumulative Wt. Retained (gm)	Cumulative %age Wt Retained (gm)	%age Passing
80mm	0.00	0.00	0.00	0.00	0.00	100.00
40 mm	0.00	0.00	0.00	0.00	0.00	100.00
20 mm	0.00	275	137.5	137.5	2.75	97.25
10 mm	170	4570	2370	2507.5	50.15	49.85
4.75 mm	4715	145	2430	4937.5	98.75	1.25
Pan	-	-	-	-	-	-

Table 9: Fineness Modulus of Proportioned Coarse Granite Aggregates

I S Sieve Designation	Wt. Retained on Sieve (10mm Agg) (gm)	Wt. Retained on Sieve (20mm Agg) (gm)	Average Weight Retained (gm)	Cumulative Wt. Retained (gm)	Cumulative %age Wt Retained ed (gm)	%age Passing
80 mm	0.00	0.00	0.00	0.00	0.00	100.00
40 mm	0.00	0.00	0.00	0.00	0.00	100.00
20 mm	0.00	225	112.5	112.5	2.25	97.75
10 mm	2432.5	4190	3311.25	3423.75	68.47	31.53
4.75 mm	1916.75	505	1210.87	4634.62	92.69	7.31
Pan	-	-	-	-	-	-

Cumulative percentage wt. retained = 163.41 + 500

$$= 663.41$$

Fineness Modulus (F.M.) = 663.41/100=6.63

Table 10: Detailed Mix Proportions for Natural and Recycled Aggregates of Marble and Granite

Mix Designation	Cement (kg/m3)	Fine aggregates (kg/m3)	Natural Coarse Aggregates (kg/m3)	Marble Coarse Aggregates (kg/m3)	Granite Coarse Aggregates (kg/m3)	Water (kg/m3)	w/c ratio
M	399	643	1157	---		192	0.48
M2	399	643	926.0	115.76	115.76	191.5	0.48
M3	399	643	810.3	173.64	173.64	191.5	0.48

M4	399	643	694.5	231.52	231.52	191.5	0.48

From the tables the fineness modulus of fine aggregates, coarse natural aggregates, marble and granite waste aggregates are 2.55, 6.6, 6.51 and 6.63.

III RESULTS AND DISCUSSION
COMPRESSIVE STRENGTH

To study the effect of replacement of natural aggregates by marble waste and granite waste aggregates used in equal proportions, cubical specimens with replacement of natural aggregates by 20% (10% marble +10% granite) , 30% (15% marble +15% granite),40% (20% marble +20% granite) were cast and tested. The results obtained for the specimen tested for compressive strength at 7 days and 28 days are reported in Table 11 and 12 respectively. The comparison of compressive strength at 7 days and 28 days for specimens with natural aggregates and the specimens containing marble and granite waste aggregates in different percentages is shown in Figure 1 and 2.

Table 11: Test Results of Compressive Strength of Specimens at 7 Days

Mix Design ation	%age Replac ement	Load (kN)	Compr essive Strengt	Averag e Compr
M1	0	473.70	21.05 / 26.19	22.87
M2	20	589.27	26.19 / 25.90	25.95
M3	30	558.00	24.80 / 24.33	25.22
M4	40	515.70	22.92 / 24.65	24.39
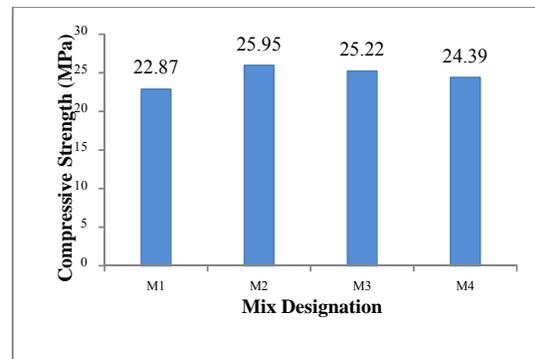
Table 12: Test Results of Compressive Strength of Specimens at 28 Days

Mix Design ation	%age Repl	Load (kN)	Compr essive Strengt	Averag e Compr
M1	0	670.50	29.78 / 28.47	29.53
M2	20	771.75	34.30 / 27.56	32.12
M3	30	745.65	33.14 / 31.52	31.15
M4	40	657.67	29.23 / 29.38	29.20

It can be seen from Tables 11, 12 and Figures 1, 2 that the compressive strength of mix M2 at 7 days and 28 days increased with replacement of natural aggregates by marble and granite waste aggregates by 20% when compared to the control mix M1. For M3 30% replacement of natural aggregates by marble and granite waste aggregates further increase in compressive strength was recorded as compared to control mix M1. For the mix M4 containing 40% replacement of natural aggregates by marble waste aggregates the decrease in compressive strength is recorded. The increase in compressive strength of concrete with replacement of natural aggregate by marble and granite waste aggregates can be attributed to improved microstructure of concrete containing marble and granite waste aggregates which may be due to higher specific surface area of marble and granite aggregates and thus improving bond in between mortar and aggregates. The decrease in percentage improvement in compressive strength at higher replacement levels may be attributed to the grading effect. Figure 3 represents the typical mode of failure of cubical specimens.

Fig. 1: Comparison of Compressive Strength of Specimens at 7 Days
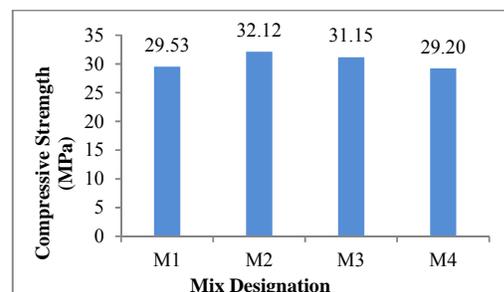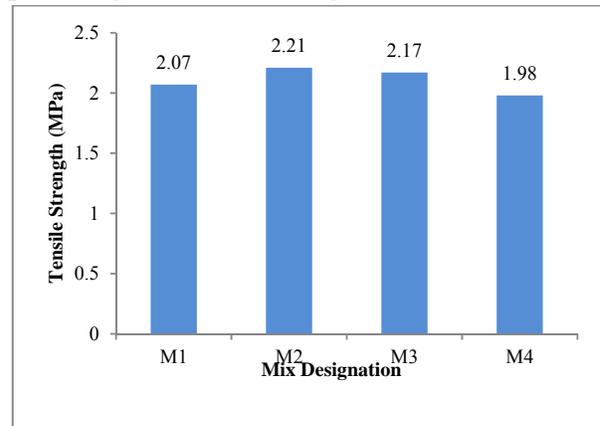
Fig. 2: Comparison of Compressive Strength of Specimens at 28 Days

Fig.3:Typical Mode of Failure for Cubical Specimens.

SPLIT TENSILE STRENGTH

To study the effect of replacement of natural aggregates by marble waste and granite waste aggregates used in equal proportions, cylindrical specimens (Series-2) with replacement of natural aggregates by 20% (10% marble+10%granite),30%(15%marble +15% granite),40% (20% marble +20% granite) were caste and tested. The results obtained for the specimen at 7 days and at 28 days are reported in Table 13 and 14.

Table 13: Test Results of Split Tensile Strength of Specimens at 7 Days

Mix Designation	%age Replacement	Split Tensile Strength (Tonnes)	Split Tensile Strength (N/mm²)	Average strength (N/mm²)
M1	0	14 14	1.98 1.98	2.07
M2	20	16 16	2.26 2.26	2.21
M3	30	16 14 16	2.26 1.98 2.26	2.17
M4	40	14 14	1.98 1.98	1.98

Table 14: Test Results of Split Tensile Strength of Specimens at 28 Days

Mix Designation	Split Tensile Strength (Tonnes)	Split Tensile Strength (N/mm²)	Average strength (N/mm²)
M1	20 22	2.83 3.11	2.92
M2	24 24	3.39 3.39	3.29
M3	24 20	3.39 2.83	3.10
M4	20 20	2.83 2.83	2.73

The comparison of compressive strength at 7 days and 28 days for specimens with natural aggregates and the specimens containing marble and granite waste aggregates in different percentages is shown in Figures 4 and 5.

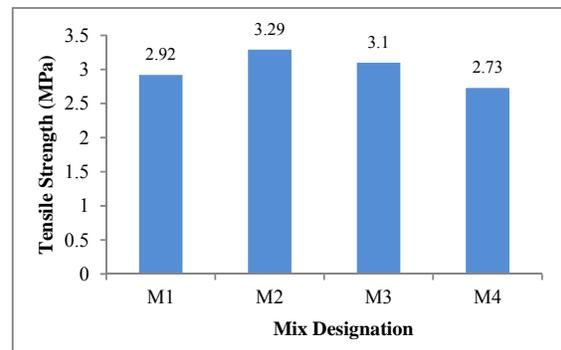**Fig. 4: Comparison of Split -Tensile Strength of Specimens at 7 Day**

Fig. 5: Comparison of Split -Tensile Strength of Specimens at 28 Days

It can be seen from above Tables 13 and 14 and Figures 4 and 5 that in line with the results obtained for compressive strength for both the series, the similar trends were obtained for split tensile strength also which correlate the beneficiary effect of replacing natural aggregates by marble waste and granite waste aggregates mixed in equal proportions.

FLEXURAL STRENGTH

To study the effect of replacement of natural aggregates by marble waste and granite waste aggregates used in equal proportions, beam specimens with replacement of natural aggregates by 20% (10% marble +10% granite), 30% (15% marble +15% granite),40% (20% marble +20% granite) were cast and tested. The results obtained for the specimen are reported in Tables 15 and 16.

Table 15: Test Result of Flexural Strength of Specimens at 7 days

Mix Designation	%age Replacement	Flexural Strength (Tonnes)	Flexural Strength (N/mm²)	Average strength (N/mm²)
M1	-	1.0 1.2	2.02 2.43	2.29
M2	2	1.4 1.3	2.83 2.63	2.76
M3	3	1.4 1.4	2.83 2.63	2.69
M4	4	1.2 1.2	2.43 2.43	2.49

Table 16: Test Result of Flexural Strength of Specimens at 28 days

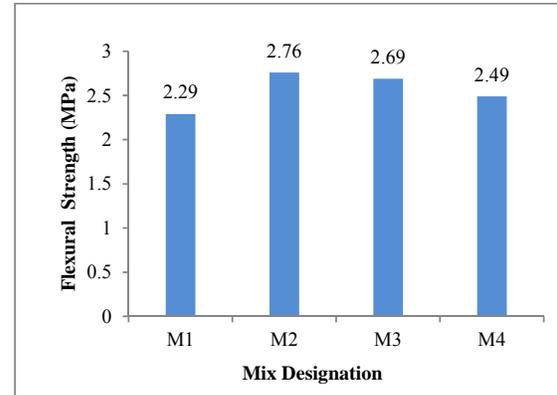| Mix Designation	%age Replacement	Flexural Strength (Tonnes)	Flexural Strength (N/mm²)	Average strength (N/mm²)
M1	-	1.8 1.9	3.64 3.84	3.70
M2	2	2.1 2.1	4.25 4.25	4.18
M3	3	1.8 2.0	3.64 4.05	3.98
M4	4	1.8 1.8	3.64 3.64	3.64

Fig. 6: Comparison of Flexural Strength of Specimens at 7 Days
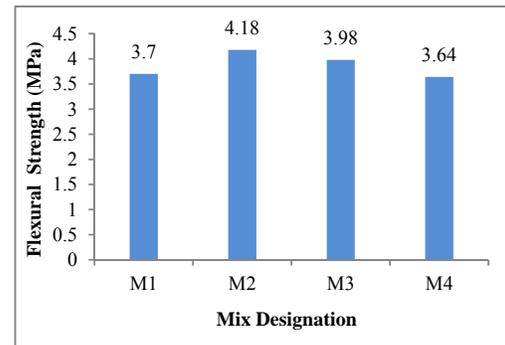

Fig. 7: Comparison of Flexural Strength of Specimens at 28 Days

It can be seen from above Tables 17 and 18 and Figures 6 and 7 that in line with the results obtained for compressive strength for both the series, the similar trends were obtained for flexural strength also which correlate the beneficiary effect of replacing natural aggregates by marble waste and granite waste aggregates mixed in equal proportions.

CONCLUSIONS

1. The compressive strength, split-tensile strength and

flexural strength of specimens tested in mixes containing marble and granite waste as recycled aggregates increased for replacement of 20% and 30%. However for the 40% replacement of marble and granite waste aggregates with natural aggregates marginal decrease in compressive strength is recorded. For mix containing 20% and 30% waste marble aggregates the compressive strength at 28 days was increased by 8.7 % and 5.5% when compared to the control mix.

2. The split tensile strength of specimens tested for mixes containing marble and granite waste as recycled aggregates increased for replacement of 20% and 30%. However for the 40% replacement of marble and granite waste aggregate with natural aggregate a marginal decrease in compressive strength is recorded. For mix containing 20% and 30% waste marble aggregates the split tensile strength is increased by 12.0% and 6% when compared to the control mix.

3. The flexural strength of specimens tested for mixes containing marble and granite waste as recycled aggregates increased for replacement of 20% and 30%. However for the 40% replacement of marble and granite waste aggregate with natural aggregate a marginal decrease in compressive strength is recorded. For mix containing 20% and 30% waste marble aggregates the flexural strength is increased by 12.9% and 7.5% when compared to the control mix.

REFERENCES

[1] Akbulut, H., Cahit, G,(2007) "Use of aggregates produced from
    marble quarry waste in asphalt pavements. Building and
    Environment",42, 1921-1930.

[2] Binici, H. etal. (2008), "Durability of concrete made with granite
    and marble as recycle aggregates" ,Journal of Materials Processing Technology 208, 299-308.

[3] IS 10262:2009 Recommended Guidelines for concrete mix
    design, Bureau of Indian Standards, New Delhi.

[1] IS 456:2000 "Indian Standards Code of Practice for plain and reinforced concrete"

(4th revision), Bureau of Indian Standards, New Delhi.

[2] IS 8112-1989. "Specifications for coarse and fine aggregates from natural sources" Bureau of Indian Standards, New Delhi,1997.

[3] IS 8112-1989. "Specifications for Ordinary Portland Cement 43 grade" Bureau of Indian Standards, New Delhi,1989.

[4] Martínez-Barrera, G., Brostow, W.(2011), " Effect of marble particle size and gamma irradiation on mechanical properties of polymer concrete"(2011), E-Polymers 61, 1-14.

[5] Pereira etal. (2009)," Influence of natural coarse aggregate size, mineralogy and water content on the permeability of structural concrete. Constr. Build. Mater"(2009). 23: 602-608.

[6] Padmini,AK,etal.(2009),"Influence of parent concrete on the properties of recycled aggregate concrete. Constr. Build. Mater", 23: 829-836.

[7] Terzi, S.(2009), " Use of marble dust in the hot mix asphalt as a filler material." Technical Journal of Turkish Chamber of Civil Engineers 14 (2),2903-2922. in Turkish.

[8] Wattanasiriwech,D.etal.(2009),"Paving blocks from ceramic tileproductionwaste".JournalofCleanerProduction17,1663-1668.

ALGORITHM FOR POWER MINIMIZATION IN SCAN SEQUENTIAL CIRCUITS

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Abstract— **The paper describes a *An ATPG* technique is proposed that reduces heat dissipation during testing of sequential circuits that have full-scan. The technique increases the correlation between successive states, during shifting in test vectors and shifting out test responses by reducing spurious transitions during test application. The reduction is achieved by freezing the primary input part of the test vector until the smallest transition count is obtained which leads to lower power dissipation. The paper presents a new algorithm which determines the primary input change time, such that maximum saving in transition count is achieved with respect to a given test vector and scan latch order. It is shown how combining the proposed technique with the recently reported scan latch and test vector ordering yields further reductions in power dissipation during test application.**

Keywords—   Scan   ,Scan   DFlip-Flop ,DFTAdvisor

I. Introduction

It is important to minimize the power dissipation in VLSI circuits to improve the reliability and reduce packaging costs. There are many techniques to reduce the power dissipation during the normal (functional) mode of operation [2, 4, 8, 12, 13, 17–19], but it is essential to examine and reduce the power dissipation during the test mode of operation due to the following two reasons. Firstly, because the power dissipated during test application is substantially higher than power dissipated during functional operation which can decrease the reliability of the circuit under test due to higher temperature and current density. Secondly, the excessive power/ground noise caused by the high rate of current flowing in power and ground lines can erroneously change the logic state of circuit lines causing some good dies to fall the test [21] leading to yield loss. Depending on level of abstraction and circuit type, high power dissipation during test application is due to the following:

a. The systems which comprise modern memory systems and multichip modules (MCMs) employ power-conscious architectural decisions where blocks are not simultaneously activated under functional operation [7]. Hence, inactive blocks do not contribute to power dissipation during the functional operation. However, when the system is in the test mode of operation, concurrent execution of tests in many blocks will result in substantially higher power dissipation when compared to functional operation.

b. Low power combinational circuits are synthesized by algorithms [2, 12, 17, 18] which seek to optimize the signal or transition probability of circuit nodes using only the spatial dependencies inside the circuit assuming the transition probabilities of primary inputs to be given. However, the complex correlations which occur at the

primary inputs must be considered [16]. The low correlation between consecutive test vectors during test application leads to substantially higher power dissipation when compared to functional operation.

c. Low power sequential circuits are synthesized by state assignment algorithms which use state transition probabilities [4, 8, 17, 19]. The state transition probabilities are computed assuming input probability distribution and state transition graph which is valid during functional operation. These two assumptions are not valid during the test mode of operation when scan design for testability (DFT) technique is employed. Furthermore, in the test mode scan registers are assigned uncorrelated values which are never reached during functional operation leading to substantially higher power dissipation.

To overcome the problem of high power dissipation during test application at the system level, a power-constrained test scheduling algorithm has been proposed for high performance memories and multichip modules [7]. The algorithm is based on a resource graph formulation for the test problem and tests are scheduled concurrently without exceeding their power ratings during test application. A new ATPG tool [21] was proposed to overcome the low correlation between consecutive test vectors during test application in combinational circuits. A different approach for minimizing power dissipation during test application in combinational circuits is based on test vector ordering [9]. To minimize power dissipation in scan sequential circuits during test application two techniques have been proposed [9, 10]. In [10], the modules and modes with the highest power dissipation are identified, and gating logic to reduce power dissipation has been proposed. Despite substantial savings in power dissipation gating logic introduces not only supplementary area overhead but also performance degradation. The technique in [9] is based on test vector and scan latch ordering increases the correlation between consecutive states during shifting in

present state part of the test vector and shifting out test responses. However, the technique proposed in [9] is test vector and scan latch order dependent and cannot significantly reduce power dissipation despite a large computational time required to explore the large design space. Furthermore, for circuits with large number of scan latches the technique pro-posed in [9] is infeasible since computational time required to compute the cost function of each solution in the large design space, is unacceptably large.

The aim of this paper is to introduce a new technique for power minimization during test application in full scan sequential circuits which eliminates the computational overhead associated with test vector and scan latch ordering [9]. The technique is based on partitioning scan latches into multiple scan chains and applying an extra test vector to primary inputs while shifting out test responses for each scan chain. This paper shows that with low test area and test data overhead high savings in power dissipation during test application in large full scan sequential circuits are achieved in low computational time.

I. The Previous work

To reduce the switching activity during scan shift, automatic test pattern generation (ATPG)-based approach and DFT-based approach were used. The advantage of the ATPG based solutions is that they do not modify the original design and the scan architecture, but modification is done on test vectors and there by power reduction can be obtained. DFT-based solutions require one to either partition the conventional scan chain architecture or insert additional hardware into the design. In Minimized power consumption for scan based Bist, extra logics are inserted to hold the outputs of all the scan cells at constant values during scan shifting. This method not only minimizes the average scan shift power, but also avoids peak power hazards during scan shifting. The main disadvantage of these approaches is the large area overhead, since additional logics are added to all the scan cells. Moreover, it may degrade circuit performance due to extra logics added between scan cell outputs and functional logics. To reduce the area overhead due to additional gates, supply gating transistors for the first-level gates at the outputs of scan cells are proposed in Low power scan design using first level supply gating. An alternative implementation

to hold the scan cell outputs by using dynamic logic was proposed in Techniques for minimizing power dissipation in scan and combinational circuit during test application. The method proposed in Inserting test points to control peak power during scan testing, inserts test points at selected scan cell outputs to keep the peak shift power at every shift cycle below a specified limit. Given a set of test patterns, logic simulation is carried out to identify the shift cycles in which peak power violations occur. Those cycles are called violating cycles. By using integer linear programming (ILP) techniques, the optimization problem is solved to select as few test points as possible such that all violating cycles can be eliminated. In Partial gating optimization for power reduction during test application, random vector simulation was used to guide partial test point selection. When simulating a random vector, the primary inputs and the pseudo primary inputs are changed to value X with pre-specified probabilities, and the number of gates becoming X after the change is used as a cost function to identify the logic value assigned at the primary inputs and the pseudo primary inputs, as well as to select scan cells to be held during scan shifting. To explore several hundred thousands of scan cells in an industrial circuit, a significant number of random vectors need to be simulated in order to choose good test points. Motivated by the test point insertion approach along with multiple scan chain, scan shift power can be reduced to a larger extend. Some scan cells have a much larger impact on toggle rates at the internal signal lines than other scan cells. These scan cells are called power sensitive scan cells. Objective is to quickly identify power sensitive scan cells and their preferred frozen values during scan shifting. By freezing a small percentage of scan cells that are the most power sensitive, reduction in scan shift power can be achieved, while minimizing the additional area overhead. Compared with the previous approaches, this approach has less area overhead and can avoid modifying scan cells at critical paths by not selecting them to freeze. This approach also provides a practical way to handle large industrial designs and since both freezing power sensitive scan cells and multiple scan chain approach is used, power can be reduced to a larger extend.

II. Power Dissipation Model

Power dissipation in CMOS circuits can be divided into static, short-circuit, leakage and dynamic power dissipation. The static power dissipation is negligible for correctly designed circuit, short-circuit power dissipation caused by short-circuit current during switching and power dissipated by leakage currents, contribute up to 20% of the total power dissipation. The remaining 80% is attributed to dynamic power dissipation caused by switching of the gate outputs [12]. If the gate is part of a synchronous digital circuit controlled by a global clock, it follows that the dynamic power P_d required to charge and discharge the output capacitance load of every gate is given by

$$P_d = 0.5 \times C_{load} \times (V_{DD}^2 / T_{cyc}) \qquad \ldots(1)$$

where C_{load} is the load capacitance, V_{DD} is the supply voltage, T_{cyc} is the global clock period and N_G is the total number of gate output transitions ($0 \rightarrow 1$ or $1 \rightarrow 0$). The vast majority of power reduction techniques concentrate on minimizing the dynamic power dissipation by reducing one or more variables of P_d. The supply voltage V_{DD} is usually not under designer control and global clock period T_{cyc} or more generally, the system throughput is a constraint rather than a design variable. Thus, node transition count (NTC)
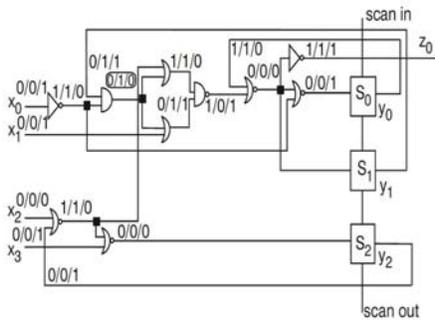
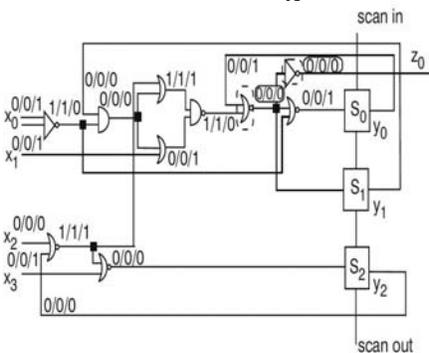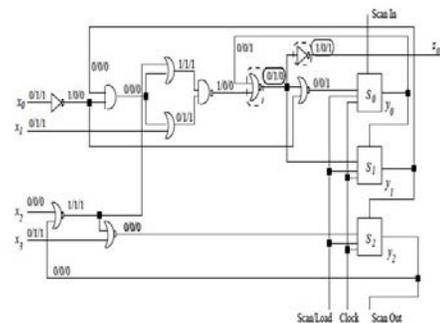$$NTC = \sum_{for\ all\ gates} N_G \times C_{load} \qquad \ldots(2)$$

a
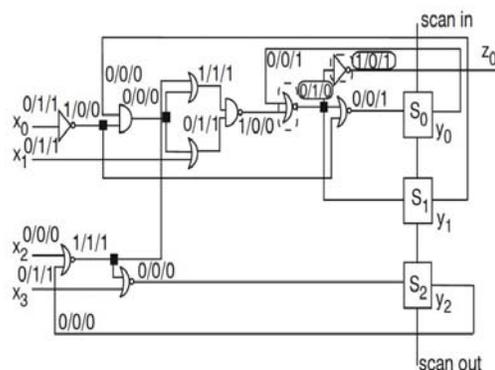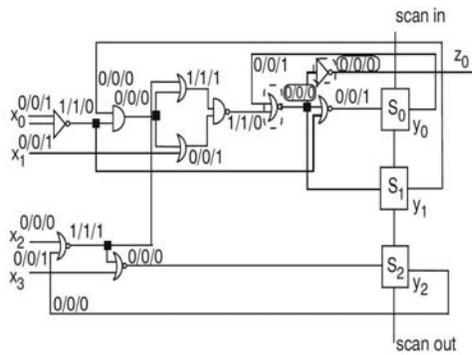
b

Fig.1Example circuit (s27 from [13]) illustrating factors which lead to spurious transitions during test application a Primary inputs change as soon as possible(ASAP) at t_0 b Primary inputs change at t_1

a

b

Fig. 2 Example circuit (s27 from [13]) illustrating factors which lead to spurious transitions during test application a Primary inputs change as late as possible (ALAP) at t_3 b Primary inputs change at t_2

is used as a quantitative measure for power dissipation throughout the paper. It has been assumed that load capacitance for each gate is equal to the number of fan-outs. The node transition count in scan latches N_{SL} is considered as in [11], where it was shown that, for input changes 0→0 and 1→1, N_{SLmin} =2, while, for input changes 0→1 and 1→0, N_{SLmax} =6

III. Minimization of Power Dissipation During Test Application By Controlling Primary Input Change Time

To motivate the need for a new test application strategy for power minimization, an overview of testing scan sequential circuits is provided. For a scan sequential circuit, each test vector $V_i = x_i@y_i$ applied to the circuit under test is composed of primary input part xi and pseudo input y_i, where @ denotes concatenation. Given m scan cells, for each test vector $V_i = x_i@y_i$ the present state part y_i is shifted in m clock cycles t_0 to t_{m-1}. In the case of partial scan sequential circuits, the non-scan cells preserve their value during clock cycles t_0 to t_{m-1}. In the next clock cycle tm the entire test vector $Vi = x_i@y_i$ is applied to the circuit under test. A scan cycle represents the $m+1$ clock cycles t_0 to t_m required to shift in the present state part of the test vector and apply the entire test vector to the circuit under test. In the following m clock cycles of the next scan cycle the test response y_0 i is shifted out simultaneously with shifting in the present state part of the next test vector $V_j = x_j@y_j$. The values of the primary inputs are important only at tm when the entire test vector is applied. Therefore the primary inputs can be changed at clock cycles t_0 to t_{m-1} without affecting test efficiency. The transitions which occur in the circuit combinational part, without any influence on test efficiency or test data, are defined as follows.

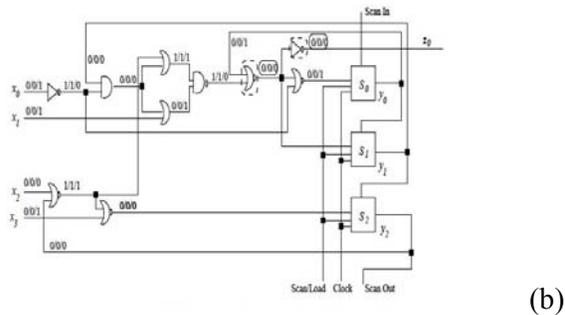(a) Primary inputs change as soon as possible (ASAP) at $t0$

Figure 3.6: Example circuit (*s27* from [23]) illustrating factors which lead to spurious transitions during test application

Definition 3.1 A spurious transition during test application in scan sequential circuits is a transition which occurs in the combinational part

of the circuit under test while shifting out the test response and shifting in the present state part of the next test vector. These transitions do not have any influence on test efficiency since the values at the input and output of the combinational part are not useful test data.

Definition 3.2 The test application strategy where primary inputs change at $t0$ is called *as soon as possible* (ASAP).
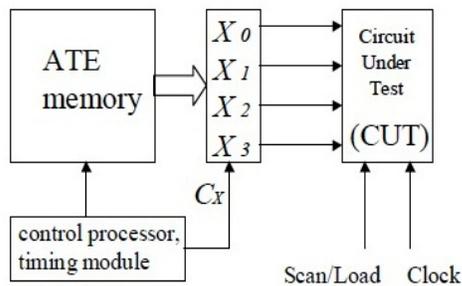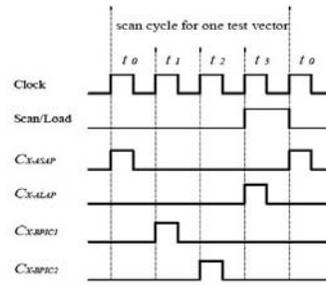
Definition 3.3 The test application strategy where primary inputs change at tm is called *as late as possible* (ALAP), where m is the number of sequential elements converted to scan cells.

Primary inputs change at $t1$

Figure 3.6: Example circuit (*s27* from [23]) illustrating factors which lead to spurious transitions during test application

Definition 3.4 The best primary input change time of test vector V_j is the time when the primary input part x_i of the previous test vector V_i changes to the primary input part x_j of

the actual test vector V_j, leading to the smallest value of node transition count during the scan cycle when test vector V_j is applied after test vector V_i. Finding the best primary input change time will lead to higher correlation between consecutive values on the input lines of the combinational part of the circuit. This leads to minimum value of *NTC* during the scan cycle, and yields savings in power dissipation.

(a) Interface to ATE

(b)

Different primary input change times

Figure 3.7: Interface to ATE for different test application strategies.

Definition 3.5 The test application strategy where best primary input change time for each test vector V_i, with $i = 0,…,n$-1, is determined such that the minimum value of node

transition count over the entire test application period is achieved, is referred to as *best primary input change* (BPIC) test application strategy.

II. Algorithm for Minimizing Power Dissipation During Test Application

This section introduces a new and exact algorithm which computes best primary input change time for each test vector with respect to a given test vector and scan cell order. We will also discuss the proposed test application strategy with the recently introduced scan cell and test vector ordering using a simulated annealing-based design space exploration leads to further reductions in power dissipation during test application.

A. Best Primary Input Change (BPIC) Algorithm

Spurious transitions induced by fixed primary input changes are solved by changing the primary inputs of each test vector such that the minimum number of transitions is achieved. For a given scan cell order with m scan cells, the total number of primary input change times is $(m+1)$. Considering n test vectors, in a given test vector order, the total number of configurations of primary input changing for all the test vectors is $(m+1)n$. Best Primary Input Change Algorithm (*BPIC-ALG*) computes the best primary input change time for each test vector for a given scan cell order and test vector order. The pseudocode of the proposed *BPICALG* algorithm is given below. The function accepts as input, a test set **S** and a circuit **C**. The outer loop represents the traversal of all the test vectors from test set **S**. All

the $m+1$ primary input change times for test vector V_i are then considered in the inner loop. For each primary input change time t_j, circuit **C** is simulated and the node transition count $NTC_{i,j}$ is registered. After the completion of the inner loop the best primary input change time t_{Bi}, for which $NTC_{i,Bi}$ is minimum, is retained and the outer loop continues until the entire test set is examined. The algorithm computes the best solution in a computational time which is polynomial in the number of test vectors n, the number of scan cells m, and the circuit size $|\mathbf{C}|$. It should be noted that *BPIC-ALG* is *test set dependent* and hence it is applicable only to *to small to medium sized* sequential circuits.

ALGORITHM: **BPIC-ALG**

INPUT: Test Set **S**, Circuit **C**

OUTPUT: Best primary input change times {**t$_{B0}$, t$_{B1}$,……., t$_{Bn-1}$**}

Node transition count over the entire test application period **NTC**

1. **NTC** $\leftarrow$ 0
2. **for** every test vector Vi from **S** with $i = 0$ **,**……, n-1 {
3. **for** every primary change time $t_{Vi} = t_j$ with $j = 0$**,**……,m
4. compute $NTC_{i,j}$ by simulating **C** during the scan cycle when applying Vi using the scan cell order {**S$_0$**,……,**S$_{m-1}$**}
5. get best primary input change time **t$_{Bi}$** for test vector V_i such that $NTC_{i,Bi}$ is minimum
6. **NTC** $\leftarrow$ **NTC**+$NTC_{i,Bi}$
7. }
8. **return** {**t$_{B0}$, t$_{B1}$,……., t$_{Bn-1}$**}, **NTC**

III. Conclusion

This paper has proposed a new technique for minimizing power dissipation in full-scan sequential circuits during test application. The technique is based on increasing the correlation between successive states, during shifting in test vectors and shifting out test responses, by freezing the primary inputs until the smallest number of transitions is achieved. A new algorithm which computes best primary input change time for each test vector has been presented. It has been shown that combining the described technique with the recently reported scan latch and test vector ordering, using a simulated annealing-based design space exploration, yields substantial reductions in power dissipation during test application. Exhaustive experimental results using both compact and noncompact test sets have shown that compact test sets have similar power dissipation during test application, with substantial reduction in test application and computational time when compared to noncompact test sets.

While this paper has shown how BPIC minimizes power dissipation in full scan sequential circuits, current research underway by the authors investigates the applicability of BPIC to partial scan and the identication of the best design for test method in terms of power dissipation during test application.

References

[1] M. Abramovici, M. Breuer, and A. Friedman. *Digital Systems Testing and Testable Design*. IEEE Press, 1990.

[2] R. Bahar, H. Cho, G. Hachtel, E. Macii, and F. Somenzi. Symbolic timing analysis and resynthesis for low power of combinational circuits containing false paths. *IEEE Transactions on CAD*, 16(10):1101–1115, Oct 1997.

[3] P. Bardell, W. McAnney, and J. Savir. *Built-In Self Test - Pseudorandom Techniques*. John Wiley & Sons, 1986.

[4] L. Benini and G. D. Micheli. State assignment for low power dissipation. *IEEE Journal of Solid-State Circuits*, 30(3):258–268, Mar 1995.

[5] F. Brglez, D. Bryan, and K. Kozminski. Combinational profiles of sequential benchmark circuits. In *Proc. Inter-national Symposium on Circuits and Systems*, pages 1929– 1934, 1989.

[6] A. Chandrakasan and R. Brodersen. *Low Power Digital CMOS Design*. Kluwer Academic Publishers, 1995.

[7] R. Chou, K. Saluja, and V. Agrawal. Scheduling tests for VLSI systems under power constraints. *IEEE Transactions on VLSI*, 5(2):175–184, Jun 1997.

[8] S.-H. Chow, Y.-C. Ho, T. Hwang, and C. Liu. Low power realization of finite state machines - a decomposition approach. *ACM Transactions on Design Automation of Electronic Systems*, 1(3):313–340, Jul 1996.

[9] V. Dabholkar, S. Chakravarty, I. Pomeranz, and S. Reddy. Techniques for minimizing power dissipation in scan and combinational circuits during test application. *IEEE Transactions on CAD*, 17(12):1325–1333, Dec 1998.

[10] S. Gerstendorfer and H. Wunderlich. Minimized power consumption for scan-based BIST. In *Proc. IEEE International Test Conference*, pages 77–84, 1999.

[11] M. Hsiao, E. Rudnick, and J. Patel. Effects of delay models on peak power estimation of VLSI sequential circuits. In
Proc. International Conference on Computer Aided Design, pages 45–51, 1997.

[12] S. Iman and M. Pedram. An approach for multi-level logic optimization targeting low power. *IEEE Transactions on CAD*, 15(8):889–901, Aug 1996.

[13] G. Lakshminarayana, A. Raghunathan, N. Jha, and S. Dey. Power management in high level synthesis. *IEEE Transactions on VLSI*, 7(1):7–15, Mar 1999.

[14] H. K. Lee and D. S. Ha. On the generation of test patterns for combinational circuits. Technical Report No. 12-93, Department of Electrical Engineering, Virginia Polytechnic Institute and State University, 1991.

[15] S. Manich and J. Figueras. Maximizing the weighted switching activity in CMOS combinational circuits under the variable delay model. In *Proc. European Design and Test Conference*, pages 597–602, 1997.

[16] R. Marculescu, D. Marculescu, and M. Pedram. Probabilistic modelling of dependecies during switching activity analysis. *IEEE Transactions on CAD*, 17(2):73–83, Feb 1998.

[17] K. Roy and S. Prasad. Circuit activity based CMOS logic synthesis for low power reliable operations. *IEEE Transactions on VLSI*, 1(4):503–513, Dec 1993.

[18] J.-M. Tseng and J.-Y. Jon. Two-level logic minimization for low power. *ACM Transactions on Design Automation of Electronic Systems*, 4(1):52–69, Jan 1999.

[19] C.-Y. Tsui, M. Pedram, and A. Despain. Low-power state assignment targeting two- and multilevel logic implementations. *IEEE Transactions on CAD*, 17(2):1281–1291, Dec 1998.

[20] A. Vital and M. Marek-Sadowska. Low-power buffered clock tree design. *IEEE Transactions on CAD*, 16(9):965–975, Sep 1997.

[21] S. Wang and S. Gupta. ATPG for heat dissipation minimization during test application. *IEEE Transactions on Computers*, 47(2):256–262, Feb 1998.

[22] Y. Zorian. A distributed BIST control scheme for complex VLSI devices. In *Proc. 11th IEEE VLSI Test Symposium*, pages 4–9, 1993.

[23] "Power Constrained Testing of VLSI circuits" by Nicola Nicolici and Bashir M. Al-Hashimi .

DDOS ATTACK DETECTION BASED ON ENSEMBLE OF NEURAL CLASSIFIER

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Abstract: **This paper reviews the detection of DDoS attck.The DDoS attacks could be detected using the existing machine learning techniques such as neural classifiers. These classifiers lack generalization capabilities which result in less performance leading to high false positives. This paper evaluates the performance of a comprehensive set of machine learning algorithms for selecting the base classifier using the publicly available KDD Cup dataset. Based on the outcome of the experiments, Resilient Back Propagation (RBP) was chosen as base classifier for our research. The improvement in performance of the RBP classifier is the focus of this paper. Detection accuracy and Cost per sample were the two metrics evaluated to analyze the performance of the RBPBoost classification algorithm. From the simulation results, it is evident that RBPBoost algorithm achieves high detection accuracy (99.4%) with fewer false alarms and outperforms the existing ensemble algorithms. RBPBoost algorithm outperforms the existing algorithms with maximum gain of 6.6% and minimum gain of 0.8%**

Keywords: DDoS Attack, Feed forward Neural Network, KDDCup dataset, Probabilistic Neural Network, Intrusion Detection, Machine Learning Techniques.

1. *Introduction:*

A distributed denial of service (DDoS) attack [1, 6] is a large-scale, coordinated attack on the availability of services of a victim system or network resources, launched indirectly through many compromised computers on the Internet. The first well-documented DDoS attack appears to have occurred in August 1999, when a DDoS tool called Trinoo was deployed in at least 227 systems, to flood a single University of Minnesota computer, which was knocked down for more than two days1. The first large scale DDoS attack took place on February 2001. On February 7, Yahoo! was the victim of a DDoS attack during which its Internet portal was inaccessible for three hours. On February 8, Amazon, Buy.com, CNN and eBay were all hit by DDoS attacks that caused them to either stop functioning completely or slowed them down significantly Our proposal is to make intelligent message discard Decisions based on Neural Networks to result in fewer false alarms.

The contributions of this paper include the following:

- Generic architecture of DDoS attack detection and response system for collaborative environment.
- Implementation of RBPBoost algorithm for the classification of network traffic.
- A classification accuracy of dataset

- 55.2% when training and testing of KDD data set.
- 55.5% when training and testing on the lab dataset.

2. Related Work
2.1. DDoS attack

DDoS attack is broadly classified into bandwidth depletion and resource depletion attack [58]. In bandwidth depletion attack, attackers flood the victim with large traffic that prevents the legitimate traffic and amplify the attack by sending messages to broadcast IP address. In resource depletion attack, attackers attempt to tie up the critical resources (memory and processor) making the victim unable to process the service. A structural approach for DDoS attack classification is proposed in [2]. The detailed analysis on DDoS attacks and available attack tools [10] show that the DDoS attack has the following characteristics:

- Source and Destination IP address and port numbers of the
- Packets are spoofed and randomly generated.
- Window size, sequence number, and packet length are fixe during the attack.
- Flags in the TCP and UDP protocols are manipulated.
- Roundtrip time is measured from the server response.
- Routing table of a host or gateway is changed.
- DNS transaction IDs (reply packet) are flooded.
- HTTP requests are flooded through port 80.

2.2. Real time feature extraction
Features are statistical characteristics derived from the collected dataset. Selection of real time feature set plays a vital role in online traffic classification. More number of features leads to better accuracy. But, computation of more number of features in real time causes more overhead and time consuming. 248 features are given and 1 feature is used to describe the class (normal or attack) in [4]. Computation of all the 248 features [1] took approximately two days on a dedicated System Area Network. Out of 248 features, some features such as maximum interpacket arrival time cannot be calculated until the entire flow is completed. Moreover, features based on Fast Fourier Transform values need better signal processing methods to reduce the computation time. So, less number of appropriate statistical features is to be selected for better pattern classification.

Feature extraction [3] is classified into two stages:

1. Feature Construction
2. Feature Selection.

Constructing the features is either integrated into the modeling process or into the preprocessing stage which includes standardization, normalization, etc. Feature Selection is divided into Filter methods and wrapper methods [5]. In filter methods, selection is based on distance and information measures in the feature space. In wrapper methods, selection is based on classifier accuracy. Three statistical features are used in [2]. Nine features are used in [3]. Flow based feature selection has been shown to block legitimate traffic in [3]. Flow based selection gives summary of metadata. By blocking the IP address and port, flow based selection does not permit the legitimate requests. Hence, instead of flow based solution, packet based solution has been used in this paper. Packet based solution minimizes the prevention of legal traffic as it blocks only the particular traffic based on the outcome of the analysis of the sequence number, window size, and packet length. Features are selected by classifying the IP flow into micro-flow and macro-flow [2]. Decision tree based Machine Learning (ML) algorithm combined with real time features has been proposed to be a good candidate for online traffic [6]. But, finding the smallest Decision Tree that is consistent with a set of training examples is NP-hard.

2.3 Ensemble of classifiers – motivation
Single classifier makes error on different training samples. So, by creating an ensemble of classifiers and combining their outputs, the total error can be reduced and the detection accuracy can be increased. There are two main components in all ensemble systems [5], viz., a

strategy to build an ensemble that is as diverse as possible and the combination of outputs of classifier for the accurate classification decisions
.Classifier combination is divided into two categories:

- Classifier selection, where each classifier is trained to become an expert in some local area of the total feature space.
- Classifier fusion, where all classifiers are trained over the same feature space.

 3.Proposed system design:

 The system is to develop an Intrusion detection system based on learning technique. Firstly known classes of intrusion like DDOS, Perl attack, Neptune attack signature is formed from standard KDD dataset. This has several string values which are not understood by the classifier. Therefore these values are converted to suitable numbers based on their properties. Database is partitioned into two parts: Training and Testing. Testing involves giving one row from the dataset as input. System classifies the row as Normal or Abnormal.

The same concept is then adopted in a real time environment to detect anomaly in internet access from college data. Router log is used to extract the features. As these features are not reclassified, we use a regression technique rather than classification to find the similarity with any data of earlier dates. Base on protocol used, we then classify the data as normal or abnormal.

The proposed system design architecture consists of the four main modules that are:

   A: data collection module:
   B: preprocessing.
   C: Classification
   D: Response

 A receiver process running in promiscuous mode captures all incoming packets and stores in data storage server. The data is stored as set of traffic flows, with each instance being described by a set of features. Each instance is expressed in vector space model (A).

 Preprocessing refers to the process of extracting information about packet connections from data and construction of new statistical features. The preprocessing steps are explained as follows:

1. Let 'x' be the input vector of dimension 'n', such that x = [x1, x2,x3, . . .xn]. The variables xi of the input vector is the original features.
2.   Let 'tx' be a vector of transformed features of dimension 'tn'

 The statically characteristics features are used to find the statistical properties such as standard deviation and variance. These features quantify the behavioral characteristics of a connection in terms of number, type of various data items with respect to time. Hence, theses features are called as statistical real time features. Seven features are used as the gradients of the vector to classify the network pattern. Normalization is a process of ensuring that each attribute value in a database structure is suitable for further querying and free from certain undesirable characteristics. Hence, each variable is normalized in the range [1, 1] to eliminate the effect of scale difference. These values are used as inputs for machine learning algorithms (B).

        In this module, Dataset of particular class is split into subsets. Each subset is trained with Ensemble of classifiers and results are combined by WMV [7]. TK is the total number of classifiers chosen using cross-validation. Cross-validation is a popular method of manipulating training data to subdivide the training data into 'k' disjoint subsets and to reconstruct training sets by leaving out some of the subsets. Results of each classification system are further combined by WPR [7]. The efficiency of classification of the classifier is significant in the decision making process. Hence, it is measured by a parameter Q-statistic. For effective decision, the Q-statistic should be zero. The training time depends on the number of times the classifier needs training which in turn depends on the mean square error between iterations reaching global minimum. The training is speeded up by removing the overlapping data and retaining only the training samples adjacent to the decision boundary. This method again consists of training and classifier is the sub stages (C). Detection system deployed in each site maintains a hash table and updates

IP address and port number (attack signature) of the suspicious blacklist nodes. When a site receives the attack signature, it checks if it exists in its hash table. If present, it means that the system is already alerted. If not, attack signature is added to the infected list. The updated attack signature is sent to all collaborating nodes, to prevent any damage that may be caused to the available services (D)
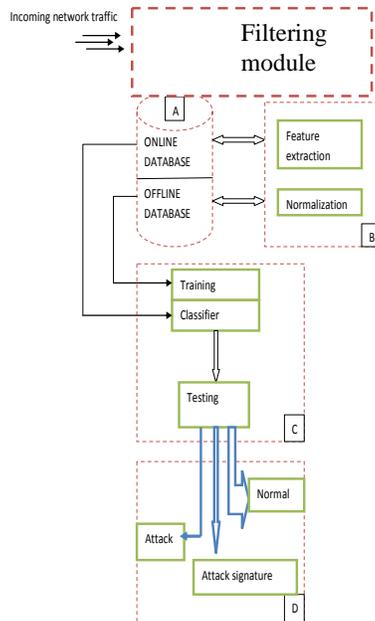

Fig 1: Architecture of ddos attack detection

4. Proposed System Algorithm:

The classification of the preprocessed data is carried out using RBPBoost algorithm. The block diagram shows that how RBPBoost algorithm uses the KDDCup99 dataset. This dataset is divided into two subset dataset and each subsets dataset is tested with this algorithm. Each subset is trained with ensemble of classifiers and results are combined by WMV [3]. TK is the total number of classifiers chosen using cross-validation. Cross-validation is a popular method of manipulating training data to subdivide the training data into 'k' disjoint subsets and to reconstruct training sets by leaving out some of the subsets. Results of each classification system are further combined by WPR [3]. The efficiency of classification of the classifier is significant in the decision making process.

The training of dataset is carried out by using feed forward neural network. But this neural network does not provide good detection accuracy. So in order to increase the detection accuracy we are used the RBP neural network

An ensemble of classifiers is trained for each individual data subset and the results are combined. A new classifier is added at each iteration. In our algorithm as given in Figure2. Two classes (Normal and DDoS attack traffic) are considered. The inputs to the algorithm are as follows:

- Training data comprised of 'n' instances with correct output labels.
- Resilient Back Propagation algorithm (RBP) as supervised base classifier.
- Number of classifier.

This dataset trained using artificial neural network and then tested with the RBP neural network to find its detection accuracy.
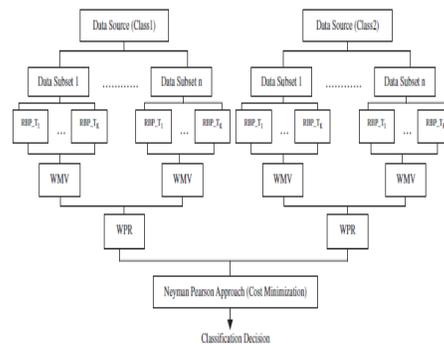

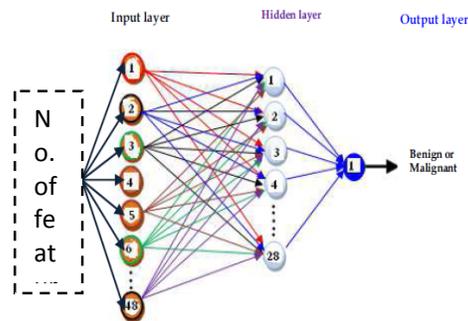Figure 2: The Block Schematic of RBP Algorithm

Figure 3: Proposed Architecture of RBP Neural Network

The purpose of the resilient back propagation (Rprop) training algorithm is to eliminate these harmful effects of the magnitudes of the partial derivatives. Only the sign of the derivative can determine the direction of the weight update; the magnitude of the derivative has no effect on the weight update. The size of the weight change is determined by a separate update value. The update value for each weight and bias is increased by a factor delt_inc whenever the derivative of the performance function with respect to that weight has the same sign for two successive iterations. The update value is decreased by a factor delt_dec whenever the derivative with respect to that weight changes sign from the previous iteration. If the derivative is zero, the update value remains the same. Whenever the weights are oscillating, the weight change is reduced. If the weight continues to change in the same direction for several iterations, the magnitude of the weight change increases.

First, investigate the storage format of the network. RBF networks are stored in objects with head RBFNet. The first component contains the parameters and the second component is a list of rules.

Initialize an RBF network with three inputs, two outputs, and five neurons. This is done by initializing a network with matrices of the appropriate size without any data.

Input:
- Training Data 'DS' of size 'N' with correct labels $y_i \in \Omega = \{y_1, y_2\}$
- Supervised algorithm base classifier
- No. of iterations or classifiers (y)
- Number of Classes (L)

Initialize:
- $\mu = 0.5$ // False Alarm Threshold
- $L = 2$

Training:
Do j = 1... L
  1. Choose samples from class 'j' and form Data Source DS_j
  2. Split DS_j into 'k' subsets $(S_1, S_2, \ldots\ldots\ldots, S_k)$
  Do m = 1.....k and t = 1......y
    a. Train S_m by supervised algorithm and obtain hypothesis h_t
    b. Compute error of h_t: $\varepsilon_t = \sum_t^h [h_t(x_i) \neq y_i]$ (4)
    c. If $\varepsilon_t > \mu$, then drop hypothesis and go to step 2.a
       Else add the classifier C_t to the Ensemble 'E_m'.
    d. Normalized error (β_t): $\beta_t = \varepsilon_t / 1 - \varepsilon_t$ $0 < \beta_t < 1$ (5)
  End
End

Testing:
Given an unlabeled instance 'X'
  A. Evaluate the ensemble 'E' of each data subset for particular class on 'X'
  B. Obtain composite hypothesis for each subset by Weighted Majority Voting
  C. Each subset's ensemble decision in combined by Weighted Product Rule
  D. Choose the class with more weights.

Figure 4: Proposed RBP Algorithm

As like the above Algorithm here we are given some specified sample of dataset to the neural network, which takes these samples and classified into its normal and attack class.

Feed forward neural network is used to create two-layer feed-forward network of neurons. Collected data and target value are considered to configure the network's inputs and outputs to match. Configuration is the process of setting network input and output sizes and ranges, input preprocessing settings and output post processing settings, and weight initialization settings to match input and target data.

The network is trained for different values of epochs and error goal, where epoch and error goal are training parameter. Typically one epoch of training is defined as a single presentation of all input vectors to the network. The network is then updated according to the results of all those presentations. Training occurs until a maximum number of epochs occur, the performance goal is met, or any other stopping condition of the training function occurs.

Implementation is carried out using MATLAB Neural Network Toolbox for the purpose DDoS attack detection. Here we implement three separate modules which are as followings

1. The first module is according to the base paper, which finds the detection accuracy of DDoS detection attack using different types of neural network with KDDCup 99 dataset input for this one.

2. The second one is the DDOS attack like matching using our college log file.

3. The final one is just shows us that how the intrusion is happened in normal wireless artificial immune system.

5. Simulation results:

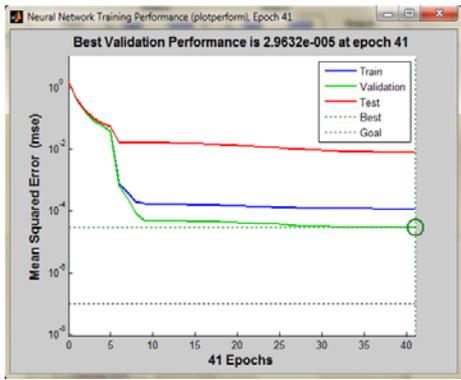After executing the neural network we got the better detection accuracy as 55.86.this we can show below.

Figure 5: Performance of the neural network showing that validation is goes on optimizing the threshold.
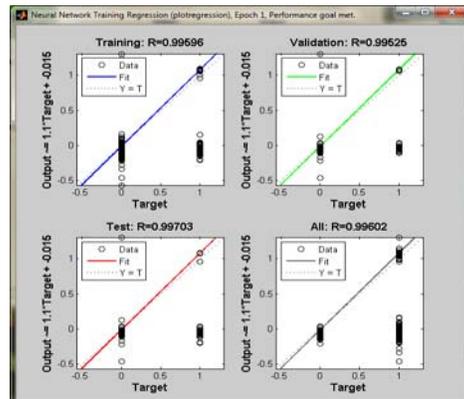

Figure 6: Training state graph showing gradient, mean deviation and validation check
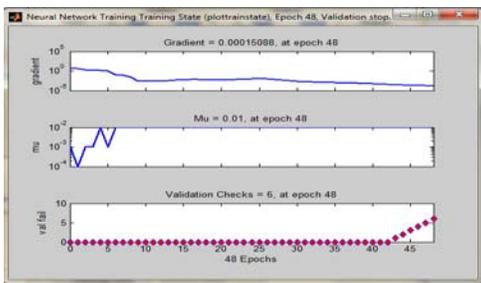

Figure 7: Error histogram of using 80 layers in the feed forward network

Figure 8: Regression graph showing the roc curve

Figure 9: shows how git college data matches with its corresponding match
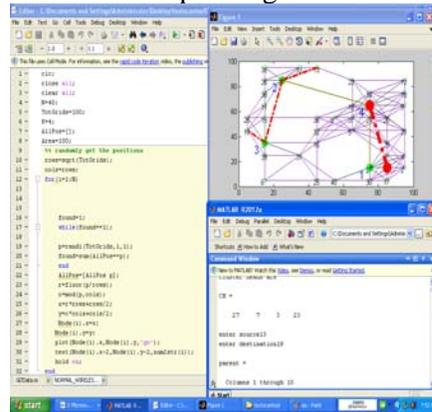
Figure 10: Shows How Intrusion Detection Is Happened In wireless AIS Network

RESULTS

Algorithm name with functions	No .of sample	Detection accuracy
Normal neural network	10000	2.88%
Best	10000	2.9623e^(-

validation		005)
Mean deviation	10000	0.01
Error rate	10000	0.08115
gradient	10000	0.00015
RBP neural network	10000	55.36%

So finally we are got the good detection accuracy. So that we are chosen RBP neural network is the base classifier.

6. Conclusion and Future Scope:

In this paper, a generic architecture for automated DDoS attack detection and response system for collaborative environment using machine learning is proposed. We have further evaluated the concept by implementing the concept in real time college data where we have used regression to suitably extract the classes from unknown pattern from college router log file. We have also defined an evolutionary technique using AIS and have applied it on simulation of Intrusion detection in mesh network where detection signature is mesh network parameters.

References:
[1] Abraham Yaar, Adrian Perrig, Dawn Song, FIT: Fast Internet Traceback, IEEEInfocomm, Mar. 2005.

[2] Alex C. Snoeren et al., Hash-Based IP Traceback, ACM Sigcomm, Aug. 2001, pp. 3–14.

[3] Alex C. Snoeren et al., Single-packet IP traceback, IEEE/ACM Transactions on Networking 10 (6) (2002) 721–734.

[4] Amey Shevtekar, Karunakar Anantharam, Nirwan Ansari, Low rate TCP denialof- service attack detection at edge routers, IEEE Communications Letters 9 (4) (2005) 363–365.

[5] Amey Shevtekar, Nirwan Ansari, A router-based technique to mitigate reduction of quality (RoQ) attacks, Computer Networks 52 (5) (2008) 957–970.

[6] Amey Shevtekar, Nirwan Ansari, Is it congestion or a DDoS attack? IEEE Communications Letters 15 (7) (2009) 546–548.

[7] Andrey Belenky, Nirwan Ansari, On IP traceback, IEEE Communications Magazine 41 (7) (2003) 142–153.

[8] Andrey Belenky, Nirwan Ansari, On deterministic packet marking, Computer Networks 51 (10) (2007) 2677–2700.

[9] Arbor Networks, Worldwide Infrastructure Security Report, Volume IV, November 2008.

[10] P. Arun Raj Kumar, S. Selvakumar, A DDoS threat in Collaborative environment "A survey on DDoS attack tools and Traceback mechanisms ", in: Proceedings of IEEE International Advance Computing Conference (IACC'09), 2009, pp.1275– 1280.

INTELLIGENT & SAFE TRANSPORTATION SYSTEM FOR MODERN DEVELOPING CITIES

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Abstract :

Road traffic congestion is a recurring problem worldwide In India, a fast growing economy, the problem is acutely felt in almost all major modern cities. This is primarily because infrastructure growth is slow compared to growth in number of vehicles, due to space and cost constraints. Secondly, Indian traffic being non-lane based and chaotic is largely different from the western traffic. The difference can be understood fully only through experience, Thus, Intelligent & Safe Transportation System (ISTS), used for efficient traffic management in developed countries, cannot be used as it is in India. ISTS techniques have to undergo adaptation and innovation to suit the contrasting traffic characteristics of Indian roads. In this position paper, we present a comprehensive study of all available ISTS systems, including both research prototypes and deployed systems. We next pose a set of interesting open research problems in the context of Indian ISTS. Finally, we list a set of public and private organizations, that play a role in Indian traffic management and research, as meaningful collaboration between field practitioners and researchers is needed for efficient transfer of relevant technology.

Though our paper focuses on the Indian traffic scenario because of our hands-on experience of working withit, many of the problems and solutions outlined in this paper.

Introduction:

Intelligent & Safe Transport Systems and Services refer to the integration of information and communication technologies with transport infrastructure to improve economic performance, safety, mobility and environmental sustainability for the benefit of all citizens. Affordable and accessible transport is clearly fundamental to sustainable health, wealth and prosperity in Modern city. It underpins employment, economic growth and global exports, while providing citizens with resources and mobility that are essential to the quality of life. The ability of transport systems to respond to mobility needs of citizens and goods is hampered by a continuous increase in traffic demand as a result of higher levels of motorization, urbanization, population growth and changes in population density. The resulting traffic Congestion reduces the efficiency of mobility systems, increasing travel times, air pollution and fuel consumption. Addressing traffic congestion was one of the

initial motivations to look at intelligent transport

Systems solutions for a better utilization of transport capacity through the exchange of real time information on infrastructure and traffic conditions. Since then, new transport applications based on information and communications technologies have emerged and continue to emerge, ranging from basic traffic management systems to management of containers; from monitoring applications such as closed-circuit television security systems to more advanced applications integrating live data and feedback from a variety of information sources (e.g. parking guidance, weather information).To meet the challenges of achieving virtually accident-free, clean and efficient mobility through ISTS, it is crucial that all elements of transport systems are able to communicate and cooperate in exchanging real-time information. Bi-directional communication is needed from vehicle to vehicle and vehicle to infrastructure. This requires the development of modern city A communication architecture that provides a common frame for cooperative systems to work together. Examples of applications based on cooperative systems that are currently under development are: traffic control and management, intersection collision warning, weather and road conditions warning, and route guidance to avoid traffic congestion. Several services of the Modern city Commission contribute to the development and deployment of ISTS in city. Transport for the Indian Commission To meet the challenges of achieving virtually accident-free, clean and efficient mobility through ITS, it is crucial that all elements of transport systems are able to communicate and cooperate in exchanging real-time information. Bi-directional communication is needed from vehicle to vehicle (V2V) and vehicle to infrastructure (V2I). This requires the development of modern technology Integrated effort essential because transport is inherently transnational in nature, research efforts to solve its problems must also transcend the scope and scale of purely national efforts. The resultant innovations should be applicable across the whole of Indian, and even beyond. Geographical continuity, standardization and interoperability of services are essential, in order to avoid the emergence of a patchwork of ITS applications and services. It is increasingly evident that technological improvements involving individual vehicles or infrastructure components and sub-systems are insufficient. Solutions must be found at the level of the interactions between the various constituents of transport systems, including users, and their optimal combination. Even with relatively small investments, the integration of existing technologies could create new services bringing more reliable, real-time traffic information and better routing.

1.1 Background of Project

Advanced Traveller Information Systems (ATIS) is one of the user services provided by ITS. With Advanced Traveller Information Systems (ATIS) information, drivers make informed decisions and are better equipped to plan their route and estimate their travel time. Route planning is an essential component of ATIS, aiding travellers in choosing the optimal path to their destinations in terms of travel distance, travel time.

In this proposal an advanced traveller information system for Pune city has been developed in GIS environment. This user-friendly system provides complete information of Hyderabad city such as road network, tourist places with in the city limits, hospitals, government and private offices, stadiums, bus and railway stations. This system provides shortest path and path to closest facility based on distance and drive time. A facility consisting of city bus routes with bus numbers, origin and destination points, and all intermediate stations have been included in the system

A sustainable transport system must provide mobility and accessibility to all urban residents in a safe and environment friendly mode of transport. This is a complex and difficult task when the needs and demands of people are not only different but also often conflicting. If a large proportion of the population cannot afford to use motorized

Transport modes – public / private – then they have to either walk or ride bicycles for their mobility. The nature of urban road traffic safety and the ways in which the

problems created by road traffic conflict need to be reviewed to promote Urban Road Safety. A particular interest is taken in the impact of road safety issues on the well being of the urban vulnerable road users. From this perspective, the study will identify and investigate the particular problems facing the urban vulnerable road users as a result of road accidents. The urban vulnerable road users may be particularly disadvantaged, as compared to   others.
Geographic Information System (GIS) usage provides spatial analysis, improved display capacities and data integration capabilities. The study will identify and highlight these issues by using GIS information system to aid policy makers and other stakeholders in their endeavour to promote Urban Road Safety.

1.2 Objectives & Scope

        The main objective of this article is to present a status report on the nature and impact of road safety in Pune city. The article highlights GIS capabilities such as special analysis tools, graphics and data integration capabilities, etc. to provide enhanced capacity for addressing urban road safety issues for vulnerable road users. The article identifies priority areas for remedial actions, enforcement issues, traffic control and traffic calming measures. The study is restricted to the urban settlement of Pune city under PMC area. The GIS will offer a platform to maintain up to date road accident database and use it for further analysis and planning. The scope of the article is to identify the characteristics of traffic accidents in Pune urban area. Developing GIS based information system will help to integrate land use information, traffic and travel characteristics, and road accident data to assess urban safety particularly for vulnerable Road users . The planning and management of urban environment require huge amount of information regarding almost all Aspects of natural and man- made features of that area. Until lately, such a study could be achieved through days of exhaustive Surveys, map generation and tedious calculations. GIS serve as a powerful tool for spatial and non-spatial analysis of data. This study tried to apply the role of GIS in the management   of urban environment.   Urban   environment basically consists of built up area, i.e.

buildings, roads, industries, but in this study try to attend to some amenities in side Pune urban activity zone. With using GIS techniques in the research we can understand how the modern technology can be used in the study of urban sprawl and its growth trend, updating and monitoring,

1.3 Introduction to Pune City

Pune is second Largest city of state the present population of Pune city is around 31, 57,000 as per 2001 census Population of Pune has increased by 56 % over the last decade in which reflects tremendous increase making it more congested than ever. The expansion process is still continuing both due to its own population expansion and the influx from surrounding areas. Understanding the growth and change brought on by urbanization is critical to those who must manage resources and provide services   in   these   rapidly   changing environments the rapid population growth has caused heavy pressure on city administration regarding issues of transportation, atmospheric pollution, water supply, sewerage, electric power and other civic amenities with impacts to the citizenry at large. Since, the provision of most civic services to the public involves geographic aspects (i.e., locate and provide) there is a logical need that all the agencies responsible for providing basic urban facilities to the citizens should have accurate maps, rectified to a common geographic reference for use in the urban environment. Intelligent Transport System (ITS) comes into picture and it holds the promise of sustainability. Intelligent Transport Systems (ITS) is the name given to the   application   of   computer   and communications technologies to transport problems. In a rapidly changing   society the emphasis on road technology improvements to assist in road management has been identified.   The   rapid   advances   in   ITS technologies have enabled the collection of data or intelligence which provides relevant and timely information to road managers and users. Keeping traffic moving is the big challenge that all levels of government are facing worldwide. Private travelers, commercial road users, and the public sector are continually searching for new and faster travel routes. Without quality and dynamic data, route selection is often a hit

and misses guessing game. The old adage, 'knowledge is power' is the obvious solution to the traffic problem. Customers want real-time information to help them select the best route to take at any given time. They need to know traffic speeds, incidents (accidents or lane closures), and road conditions. With Advanced Traveler Information Systems (ATIS) information, drivers make informed decisions and are better equipped to plan their route and estimate their travel time. Fast and accurate information translates into several benefits for ATIS customers such as reduction in travel time, reduction in stress levels, the avoidance of congestion, and perhaps the most important benefit, the avoidance of unsafe driving conditions.

1.4 Case of Pune City

Pune city is an important urban center in Maharashtra and a rapidly growing metropolis of the country. The metropolitan area of Pune extends over 809 sq km. The Pune Metropolitan Area (PMA) consists of Pune Municipal Corporation (PMC), the Pimpri-Chinchwad Municipal Corporation (PCMC), Cantonment Boards of Pune and Kirkee and some villages. The total length of road network in PMC area is about 1800kms. The importance of Pune as an industrial centre has grown rapidly since the 1960's when industrial expansion in Mumbai region was curtailed. Consequently Pune has become a major centre in the state, having attracted engineering industry such as motorvehicle manufacturing plants buses, cars and motorcycles. In addition to this, a number of multi-national companies have manufacturing bases within the city. Much of the local industry is concentrated along the main Pune-Bombay highway, enabling manufactured goods to be dispatched. As per 2001 census population of the Pune city is a home to 26 lakhs people and 1.5 lakh vehicles. For the last two decades Pune has registered a steep growth in number of public-private vehicles. But the road infrastructure and the utilities have not expanded in commensurate with increase in number of vehicles. The city manifests all the problems of a metropolis like increase in traffic congestion, speed reduction, environmental pollution high incidence of road accidents and degradation of quality of life. The problem of road accidents has been brought out by an unprecedented growth in motorized vehicles which is further aggravated by the interstate truck movement that cuts through the Pune city.

The growth of vehicles in Pune has assumed extraordinary proportions, especially in the case of two wheelers. So far there are about 15.6 lakh vehicles registered in PMC and PCMC area out of which more than 12 lakh vehicles are two wheelers.

Public transport has always been a hallmark of good transportation system. Commuters in Pune are heavily dependent on the personalized mode of transport like two wheelers and the public transport has always taken a back seat. Maxuimum number of accidents occurs from 0900 to 1300 hrs in the morning and 1800 to 2200 hrs in the evening. Two wheelers, three wheelers and cars are involved in maximum number of accidents. Two wheeler riders alone are involved in more than 45% of fatal accidents and 39% of the fatal accident victims are pedestrians. Thus pedestrians and two wheeler riders in Pune city are the most vulnerable road users exposed to high risk of road accidents on Pune city roads.

Pune district is located between $17°$ 54' and $10°$ 24' North Latitude and $73°$ 19 and 75 10' East Longitude, The district is bound by Ahmadnagar district on the north-east, Solapur district on the south-east, Satara district on south. Raigad district on the west and Thane district on the north-west Pune district forms a part of the tropical monsoon land.

1.5 Road Network

Pune district is well connected with the state capital and surrounding headquarters through road and rail linkages. The road network consists of Express Highway, National Highways, State Highways and Major District Roads. The district has total length of 13.642 km of roads. Following National Highway pass through the district:

1. National Highway No. 4 (Mumbai-Bangalore)
2. National Highway No. 9 (Pune-Solapur-Hyderabad)
3. National Highway No. 50 (Pune-Nashik).

1.6 Rail Network

The district has a total rail network of 311 km. Pune and Daund are the two major junction stations. Following are the two main railway routes pass through the district:

1. Mumbai-Pune-Solapur
2. Pune-Miraj

1.7 Air Route

Pune is well connected through domestic airlines with the entire country The airport located at Lohgaon has recently acquired status of an international airport. Also it is proposed to develop an International air-cargo hub near Khed Tahsil of the district.

1.8 Demographic Profile

The total population of the study area in 2001 was 35.6 lakhs. The decadal growth in PCMC area is almost 100% in the past 3 decades. PMC area has registered an average Decadal growth of around 35% and a decline in population is observed in both the cantonments. The estimated population figures of study area for the base year 2008.

Table 1: Demographic Profile Estimation

1.9 Significance of the study

The planning and management of urban environment require huge amount of information regarding almost all Aspects of natural and man- made features of that area. Until lately, such a study could be achieved through days of exhaustive Surveys, map generation and tedious calculations. GIS serve as a powerful tool for spatial and non-spatial analysis of data. In This study tried to apply the role of GIS in the management of urban environment. Urban environment basically consists of built up area, i.e. buildings, roads, industries, but in this study try to attend to some amenities in side Pune urban activity zone.With using GIS techniques in the research we can understand how the modern technology can be used in the study of urban sprawl and its growth trend, updating and monitoring, Using repetitive coverage, urban environment especially land use the study on Pune Municipality .Selection of Study Area Pune city

in India, growing at a very fast rate, and PMC area in pune spread over 243.84 SqKm.

Regio	2011	2021	2031
PMC	3115431	4807868	5443642
PCM	1729320	1915320	2106123
Pune	67861	88603	93134
Khad	77417	85600	89977
Total	4992040	6899412	7734907

94% increase in area from 1961 to 2001,Population grown 400 times from 1961 to 2001,CAGR for 1991- 2001 is 4.94% and 50% of population growth in last decade due to in-migration. Aims and Objectives: The precise aim to this present study is to find out different amenities in PMC area and suggest planning to provide better utility services. Role of Geographic Information System The 19th century witnessed a trickle of urbanization and the emergence of metropolises. To control the world's urban development as crucial for the future of humanity.

1.10 Selection of Study Area

Pune city in India, growing at a very fast rate, and PMC area in pune spread over 243.84 SqKm. 94% increase in area from 1961 to 2001, Population grown 400 times from 1961 to 2001, CAGR for 1991-2001 is 4.94%and 50% of population growth in the decade dueto in migration Aims and Objectives: The precise aim to this present study is to find out different amenities in PMC area and suggest planning to provide better utility services.

Conclusion

Traffic congestion is an important problem in Indian cities. The characteristics of Indian roads and traffic make the problem interesting to solve. There is scope for evaluating existing ideas in different and challenging traffic scenarios, innovate new solutions and empirically evaluate ideas in collaboration with public and private sectors. In this paper, we make a small effort to put together the different ideas and people relevant in Indian ISTS, so that it gives an overview of the problem and the available solutions and outlines a set of open questions to answer.

References

[1]   http://www.cse.iitb.ac.in/~riju/   [2] http://paleale.eecs.berkeley.edu/~varaiya/transp. html.

[3]   http://www.scats.com.au/index.html.   [4] http://www.visioway.com,http://www.traficon .com.kyunqueue.   [5]Intelligent Transport Systems for Indian Cities Rijurekha Sen, Bhaskaran Raman {riju, br}@cse.iitb.ac.in

AN EFFICIENT TECHNIQUE FOR ROUTING IN WIRELESS SENSOR
NETWORK

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Abstract -
Wireless Sensor Networks have gained popularity due to the fact that they offer low-cost solutions for a variety of application areas, but effective defence against security attacks is a challenging physically insecure environment. Although significant research effort has been spent on the design of trust models to detect malicious nodes based on direct and indirect evidence, this comes at the cost of additional energy consumption. Various secured routing protocols have been developed with the help of cryptographic techniques in order to protect the network against the compromised nodes. However the routing protocols that use encryption schemes require large memory for storing the keys and more computation. The multi hop routing in Wireless Sensor Networks offers little protection against identity deception through replaying routing information. To secure the wireless networks against adversaries misdirecting the multi hop routing, a robust for routing in wireless sensor networks has been developed. The proposed technique uses distance, trust and energy as metrics when choosing the best path towards the destination.

task. A sensor network consists of large number of densely deployed sensor nodes with limited energy and computation. The sensor nodes are susceptible to various types of attacks, since they operate in a

Keywords - Wireless Sensor Networks, routing protocol, trust, energy, security

I. INTRODUCTION

Wireless sensor network (WSN) [2] consists of spatially distributed autonomous sensors to monitor physical or environmental conditions, such as temperature, sound, pressure, etc. to cooperatively pass their data through the network to a main location. A WSN is composed of tens to thousands of sensor nodes, which are low-power, low-cost, small, resource-constrained devices. Using a narrow radio communication range, a sensor node wirelessly sends messages to a base station via a multihop path.

WSNs are used in critical applications like military surveillance, homeland security and medical monitoring, and, in these cases, protecting the network against malicious attacks is crucial. However, WSNs have unique characteristics: wireless transmission medium, limited resources available on sensor nodes, hostile environment, adhoc deployment,

unreliable communication, and unattended operation. Therefore, protocols for critical sensor networks should be designed with security in mind, while taking into consideration their specific constraints and challenges. For large sensor networks, multi-hop communication is more energy-efficient than single-hop communication. The multihop routing of wireless sensor networks often becomes the target of malicious attacks. An attacker may tamper nodes physically, create traffic collision with seemingly valid transmission, drop or misdirect messages in routes, or jam the communication channel by creating radio interference [3].

As a harmful and easy-to-implement type of attack, a malicious node simply replays all the outgoing routing packets from a valid node to forge the latter node's identity. The malicious node then uses this forged identity to participate in the network routing, thus disrupting the network traffic.

It leads to several kinds of attacks like Selective Forwarding, Wormhole, Sinkhole and Sybil attacks [4]. The routing packets, including their original headers, are replayed without any modification. Even if this malicious node cannot directly overhear the valid node's wireless transmission, it can collude with other malicious nodes to receive those routing packets and replay them somewhere far away from the original valid node, which is known as a wormhole attack. A node in wireless network usually relies solely on the packets received to know about the sender's identity, replaying routing packets allows the malicious node to forge the identity of this valid node. After "stealing" that valid identity, this malicious node is able to misdirect the network traffic. For instance, it may drop packets received, forward packets to another node not supposed to be in the routing path, or even form a transmission loop through which packets are passed among a few malicious nodes infinitely. It is often difficult to know whether a node forwards received packets correctly even with overhearing techniques. Sinkhole attacks are another kind of attacks that can be launched after stealing a valid identity. In a sinkhole attack, a malicious node may claim itself to be a base station through replaying all the packets from a real base station. A fake base station thus could lure more than half the

traffic, creating a "black hole." The same technique can be employed to conduct another strong form of attack—Sybil attack: through replaying the routing information of multiple legitimate nodes, an attacker may present multiple identities to the network. A valid node, if compromised, can also launch all these attacks.

Most routing protocols for sensor networks use a single metric to determine the best path to destination. Some use two metrics such as location and energy [5], [6], location and trust [7], or trust and link quality [8]. Hence there is a need for a routing framework that can be easily extended to support any metric.

In this paper, we propose a trust and energy-aware, location-based based technique for routing in WSN's. The method uses trust values, energy levels and location information in order to determine the best paths towards a destination. The protocol achieves balancing of traffic load and energy, and generates trustworthy paths when taking into consideration all proposed metrics

II. RELATED WORK

Based on the network structure, routing in Wireless Sensor Networks can be classified in flat-based, hierarchical based and location-based routing [9]. Based on protocol operation, routing protocols can be classified in multi-path based, query-based, negotiation-based, QoS-based and coherent-based routing protocols.

The relevant routing protocols, which take into consideration trust values when determining the path to the, destination are listed below:

T. Ghosh, N. Pissinou, and K. Makki [10] introduced the Trust-embedded AODV (T-AODV) routing to secure the ad hoc network from independent malicious nodes by finding a secure end-to-end route. When a node wants to find a route to another node, it initiates a route discovery by broadcasting a route request (RREQ) packet. The packet header contains a trust level field, in addition to the other fields in AODV RREQ. When an intermediate node receives the RREQ packet, it rebroadcasts it after modifying the trust level field to include the trust level of the node that sends it the RREQ. Every node checks back the rebroadcasted RREQ packet from its next node to see whether it has provided the proper information. If not, it immediately broadcasts a warning message

questioning the trustworthiness of that node. This protocol does not encourage any intermediate node to send a route reply (RREP). The final route selection is based upon the trust level metric. Hop count plays a role in deciding the final route only when more than one packet has same trust level. The RREP packet has the next hop information. The protocol tries to finds a secure end-to-end path free of malicious nodes and can effectively isolate a malicious entity trying to attack the network independently or in collusion with other malicious entities

A. Rezgui and M. Eltoweissy [11] proposed a routing procedure called Trust Aware Routing Protocol (TARP). It is responsible for routing messages from the different nodes to the base station. TARP is a trust-based routing scheme. Trust refers to the confidence that a node has in a neighbor's cooperation. A node's cooperation, in this context, is the likelihood that it forwards its neighbors' messages. TARP is based on the basic idea of avoiding to route through non cooperative nodes. The intuition is that sending packets to nodes that are not likely to cooperate in routing messages to their neighbors would probably waste energy with no payoff. TARP captures the concept of cooperation in terms of "routing reputation". Informally, reputation is a perception that a node has regarding another node's cooperation. TARP consists of two concurrent phases: (i) reputation assessment and (ii) path reliability evaluation

Z. Cao, J. Hu, Z. Chen, M. Xu, and X. Zhou [12] introduced a routing scheme called Feedback Based Secure Routing protocol (FBSR) for wireless sensor networks. It utilizes feedback information from neighbor nodes to represent the current states of them. On transmission of a packet, the sender prioritizes its neighbors with an evaluation function and places this neighbor list in the packet header. Neighbors, on receiving the packet, will includes its feedback in the ack frame and acknowledges the sender, and in the meantime makes independent decision of whether to forward the packet. FBSR consists of local independent forwarding decisions based on current feedback information and prediction of future conditions. Without any cryptographical protection, the stateless FBSR is resilient to routing state corruption, Wormhole and HELLO flood attacks. To protect FBSR from routing attacks such as Sinkholes and Sybil attacks, we propose

the Keyed One Way Hash Chain (Keyed-OWHC) to authenticate the feedback from neighboring nodes.

T. Zahariadis, H. Leligou, P. Karkazis, P. Trakadas, I. Papaefstathiou, C. Vangelatos, and L. Besson [13] proposed a location-based trust-aware routing solution called Ambient Trust Sensor Routing (ATSR). It incorporates a distributed trust model which relies on both direct and indirect trust information to protect the WSN from a wide set of routing and trust-related attacks. The routing and trust overhead introduced by ATSR includes the Beacon (broadcast) message which is used by each node to periodically announce its location coordinates, node id and remaining energy, the reputation request (multicast) message used to periodically request indirect trust information and the reputation response (unicast) message which is used to provide indirect information as a reply to a reputation request message.

Most existing routing protocols for WSNs either assume the honesty of nodes or focus on energy efficiency [14], or attempt to exclude unauthorized participation by encrypting data and authenticating packets. Below are some of the examples of these encryption and authentication schemes for WSNs:

A. Perrig, R. Szewczyk, W. Wen, D. Culler, and J. Tygar [15] proposed SPINS: Security Protocols for Sensor Networks. SPINS includes two building blocks: SNEP and μ*TESLA*. SNEP provides data confidentiality, two-party data authentication, and data freshness for peer-to-peer communication (node to base station). μ*TESLA* provides authenticated broadcast. Each node shares a secret key only with the Base Station and not with any other nodes. Furthermore, the routing tables are calculated by the sink and disseminated to the sensors. The protocol constructs two alternative disjoint paths between each sensor node and the sink. Each message sent from a source to a destination is sent multiple times through each alternative path. The one-way hash chain proposed in μTesla is used to authenticate messages sent by the BS and appropriate MAC mechanisms are implemented to verify the integrity of the packets.

C. Karlof, N. Sastry, and D. Wagner [16] proposed TinySec the first fully-implemented link layer architecture for Wireless Sensor Networks. TinySec supports two different

security options: authenticated encryption (TinySec-AE) and authentication only (TinySec-Auth). With authenticated encryption, TinySec encrypts the data payload and authenticates the packet with a MAC. The MAC is computed over the encrypted data and the packet header. In authentication only mode, TinySec authenticates the entire packet with a MAC, but the data payload is not encrypted.

R. Watro, D. Kong, S. Cuti, C. Gardiner, C. Lynn, and P. Kruus [17] proposed Tinypk: Securing Sensor Networks with Public Key Technology. This security scheme is a mechanism for providing authentication and key exchange between an external party and a sensor network. TinyPK is based on the well-known RSA cryptosystem. All that is required to perform a TinyPK 1024-bit basic public operation is to cube a 1024-bit number and to take its residue modulo a large prime.

In addition to the cryptographic methods, trust and reputation management has been employed in generic ad hoc networks and WSNs to secure routing protocols. Basically, a system of trust and reputation management assigns each node a trust value according to its past performance in routing. Then such trust values are used to help decide a secure and efficient route. However, the proposed trust and reputation management systems for generic ad hoc networks target only relatively powerful hardware platforms such as laptops and smartphones [18], [19], [20], [21].

The proposed protocol is a location-based routing protocol, because it uses the location of neighbor nodes for determining the best path towards the destination. However, it also considers trust and energy when determining the best next hop. In addition, the protocol uses trust values to determine whether to forward packets from specific nodes.

III. DESIGN

The Trust and Energy-aware Framework Routing is a trust and energy-aware, location-based routing protocol for Wireless Sensor Networks. It includes two phases: setup and forwarding. In the first phase, the best next hop towards the base station is selected by taking into consideration several factors, such as trust, energy and location. In the second phase, the packets generated by trustworthy nodes are forwarded using the selected next hop.

By evaluating trust value of neighboring nodes, the method secures the multi-hop routing in WSNs against attacker misdirecting the routing path. It determines such an attacker by their low trust values. There are several notations are used, they are

Neighbor: For a node N, neighboring node of N is reachable from N with one hop wireless transmission.

Distance: The distance between two nodes is measured using Euclidean distance formula.

Trust Rule: The trust rule defines the trustworthiness of each node based on several criteria such as bandwidth consumption, packet drops etc.

Energy cost: For a node N, the energy cost of a neighbor is the average energy cost for successfully deliver a unit sized data packet from current node to next hop node.

The technique secures the multi-hop routing in WSNs against intruders misdirecting the multi-hop routing by evaluating the trustworthiness of neighboring nodes. The Trust Manager identifies such intruders by their low trustworthiness and routes data through paths circumventing those intruders to achieve satisfactory throughput. It integrates location, trustworthiness and available energy in making routing decisions. For a node N to route a data packet to the base station, N only needs to decide to which neighboring node it should forward the data packet. Once the data packet is forwarded to that next-hop node, the remaining task to deliver the data to the base station is fully delegated to it, and N is totally unaware of what routing decision its next-hop node makes. To choose its next-hop node, N considers both the trustworthiness and energy of its neighbors. For that, N maintains a neighborhood table with trust level values and energy levels for certain known neighbors.

The Energy Watcher is responsible for recording the Energy Cost for each known neighbor based on node N's observation of one-hop transmission to reach its neighbors and the energy cost report from those neighbors. A compromised node may falsely report an extremely low energy cost to lure its neighbors into selecting this compromised node as their next-hop node which is tracked by Trust

Manager. Trust Manager is responsible for tracking trust level values of neighbors based broadcast messages from the base station about data delivery. Once N is able to decide its next hop neighbor according to its neighborhood table, it sends out its energy report message: it broadcasts to all its neighbors its energy cost to deliver a packet from the node to the base station.

Consider the Figure 1 in which node A, B, C and D are all honest nodes and not compromised. Node A has node B as its current next-hop node while node B has an attacker node as its next-hop node.
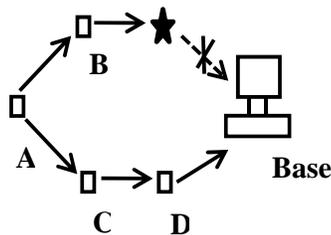
Figure 1: Working of Trust

A. Routing Procedures

In WSNs, the source node will send detected event of interest to base station through some intermediate nodes. This is the function of multihop routing. In order to maintain stability in routing path, the node will maintain same next hop until next new broadcast message from the base station is occurred. At the same time to reduce the traffic in network, their energy cost reports of that next hop node do not occur until broadcast from base station is changed. If a node does not choose next hop node until next new broadcast message from base station, it will provide guarantee for all path as a loop free path. A node will change their next hop node when their chosen next hop node will receive and deliver data properly.

The attacker drops every packet receives and thus any data packet passing node A will not arrive at the base station. After a while, node A discovers that the data packets it forwarded did not get delivered. The Trust Manager on node A starts to degrade the trust level of its current next-hop node B although node B is absolutely honest. Once that trust level becomes too low, node A decides to select node C as its new next-hop node. In this way node A identifies a better and successful route (A – C – D – Base Station).

B. Selection of Routing Path

Each node in WSNs will select the next hop node based on their neighborhood table by considering energy cost and trust value of that node. The node will eliminate attacker node that misdirect traffic by replaying routing information. For node N in WSNs will select the route for sending data to destination such as base station with optimal next hop node from that neighboring node by considering trust level and energy cost and finally forwarded the data to chosen next hop node immediately. Among the remaining neighboring nodes will select next hop node through by evaluating their energy consumption and reliability for successful delivery of packets. Therefore a node will select next hop node with high trust values, it's automatically protects the network from an attacker who forges the identity of an attractive node such as base station. The energy driven route is achieved when each node in WSNs will choose their neighbors in terms of energy.

C. Trust Manager

Trust, or the trust on the behaviour of the elements of the network, is a key aspect for WSN. A trust management system can be useful for detecting a node which is not behaving as expected (either faulty or maliciously) or it can assist in the decision-making process, for instance, if a node needs a partner in order to achieve a common goal.

Each node in WSNs will select the next hop node based on their neighborhood table by considering energy cost and trust value of that node. The node will eliminate attacker node that misdirect traffic by replaying routing information. For node N in WSNs will select the route for sending data to destination such as base station with optimal next hop node from that neighboring node by considering trust level and energy cost and finally forwarded the data to chosen next hop node immediately. Among the remaining neighboring nodes will select next hop node through by evaluating their energy consumption and reliability for successful delivery of packets. Therefore a node will select next hop node with high trust values, it's automatically protects the network from an attacker who forges the identity of an attractive node such as base station. The energy driven route is achieved when each node in WSNs will choose their neighbors in terms of energy. Here

the threshold of battery power is set to 50. A node that has lost its energy below the threshold is not included in transmission.

The Trust Manager keeps track of the trust levels of every node in the network. Suppose if a node tries to enter into the network through identity deception and performs illegal activities that either halt the transmission process or misdirect the data transmission are immediately identified and are reflected in the trust table. However, once the malicious node has been identified the transmission is not stopped but an alternative minimum hop path is taken for routing purpose.

D. Energy Watcher

When sensor nodes forwards messages in the network they use their energy in forwarding mechanism but at some point when node depletes it's all energy it fails to transmit further messages resulting in loss of data. Usually, the closest neighbor node will be heavily utilized in routing and forwarding messages while the other nodes are less utilized. This uneven load distribution results in heavily loaded nodes to discharge faster when compared to others. This causes the failure of few over-utilized nodes which results in loss of data, resulting in increase of failed messages in the network. The Energy Watcher takes care of this to minimize the data loss and maximize the lifetime of the network.

The Energy Watcher works on forwarding rule based on location and energy levels of nodes. Each node knows its own geographic location and its own energy levels as well as the location and energy level of its neighbors. The transmitting node writes the geographic position of destination into the packet header and forwards it to the neighbor which is alive (having energy level above than the set threshold) and has the minimum distance among those neighbors having the maximum energy level. In this regime, packet transmission will go on and each node chooses its next hop by following the specified routing technique. This procedure repeats until the packet reaches the destination node.

Packet can terminate in two ways (i.e. successful termination and unsuccessful termination). In successful termination, packets reach to the destination node. While in unsuccessful termination, there are two possibilities. Either destination node is dead or

the packet reaches to a node which has no neighbor alive to forward the packet so in this case the packet will drop.

A simple energy model has been used in which every node starts with the same initial energy and forwards a packet by consuming one unit of energy. Initially, all nodes have energy level equal to 100 joules. Each node depletes energy in transmitting and receiving one packet which is equal to 0.1 joule.

IV. SIMULATION

The nodes are randomly placed in a 600 x 600 m^2 field area. The sensor nodes are immobile, so every sensor node is static. Initially, each node has same energy level as specified in energy model. Any node having energy less than or equal to set threshold will be considered as dead. The battery of each node is consumed at the time of sending and receiving packets and at the time of idle state, and it is impossible to communicate when the battery is empty. Total simulation time is 100 seconds. The different simulation parameters that are set are described in the below Table 1.

Simulation	Values
Simulator	NS 2.34
Geographical area	600 x 600
Number of nodes	30
Channel type	**Wireless Channel**
Radio-propagation	Two Ray Ground
MAC type	802.11
Queue type	DropTail/PriQueue
Link layer type	LL
Antenna type	Omni Antenna
Simulation time (s)	100

Table 1: Simulation Parameters

The following are some of the performance metrics evaluated to analyze the simulation results:

Packet Delivery Ratio (PDR) is defined as the ratio of data packets received by the destinations to those generated by the sources. Mathematically, it can be defined as:

PDR= (S1/S2)* 100

Where, S1 is the sum of data packets received by the each destination and S2 is the sum of data packets generated by the each source. The graph shows the fraction of data packets that are successfully delivered during simulation time

versus the number of nodes. The Snapshot 8.10 highlights the relative performance of existing method without Trust and Energy metrics and with Trust and Energy metrics for Packet Delivery Ratio with varying numbers of nodes of 10,15,20 etc. It is observed that implemented method has a higher Packet Delivery Ratio compared to the existing method.
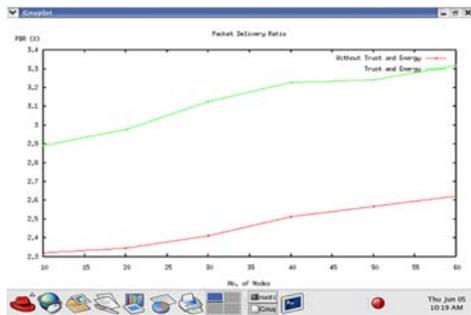

Figure 2: Packet Delivery Ratio

End to end delay is defined as the average time it takes a data packet to reach the destination. This includes all possible delays caused by buffering during route discovery latency, queuing at the interface queue. This metric is calculated by subtracting time at which first packet was transmitted by source from time at which first data packet arrived to destination. Mathematically, it can be defined as:

Avg. End to end delay= (S/N)

Where S is the sum of the time spent to deliver packets for each destination, and N is the number of packets received by the destination nodes. The Snapshot 8.11 highlights the relative performance of existing method without Trust and Energy metrics and with Trust and Energy metrics Average End To End delay with varying numbers of nodes of 10,15,20,25 etc. It is observed that implemented method has a lower End to End Delay compared to the existing method.
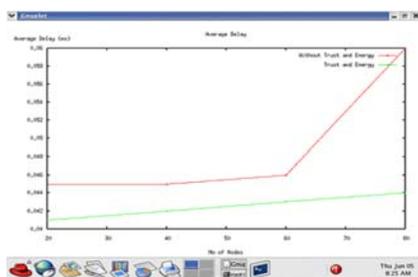
Figure 3: End to End Delay

V. CONCLUSION AND FUTURE WORK

Wireless Sensor Networks that are used for deploying critical applications such as military surveillance or medical monitoring requires the need to provide a high level of security and trustworthiness. Therefore, routing protocols for WSNs should be designed with security in mind, taking into account multiple metrics that support network availability.

The Trust and Energy-aware framework for Routing is a location-based, trust and energy-aware routing mechanism for wireless sensor networks. It uses several metrics: trust values, energy levels, the distance between the local and the neighbor node, and the distance between the neighbor node and the destination. The neighbor with the lowest cost is chosen as next hop towards the base station. The Trust and Energy-aware framework for Routing has two phases: the Setup and the Forwarding phase. In the Setup phase, the next hop is determined, and in the Forwarding phase, the packets generated by trustworthy nodes are forwarded using the selected next hop. It achieves a good balancing of load and energy, and generates trustworthy paths. The implemented technique achieves a higher packet delivery ratio and lower end to end delay.

The future work can address the fact that when the number of isolated malicious nodes increases, some nodes may find them totally surrounded by malicious neighbors and cannot participate effectively in the network. Several mechanisms may be used to solve this issue. One possible solution can be making the nodes that are totally surrounded by malicious neighbors adjust dynamically their belief and disbelief thresholds. Another solution is to give malicious nodes a chance to repent, by letting them broadcast repent packet to their 1-hop neighbors, which can place them on a probation period before deciding whether to forgive them or not.

VI. REFERENCES

[1] G. Zhan, W. Shi, and J. Deng, "Tarf: A trust-aware routing framework for wireless sensor networks," in *Proceeding of the 7th European Conference on Wireless Sensor Networks (EWSN'12)*, 2012.

[2] F. Zhao and L. Guibas, *Wireless Sensor Networks: An Information Processing*

Approach. Morgan Kaufmann Publishers, 2004.

[3] A. Wood and J. Stankovic, "Denial of service in sensor networks," *Computer*, vol. 35, no. 10, pp. 54–62, Oct 2002.

[4] C. Karlof and D. Wagner, "Secure routing in wireless sensor networks: attacks and countermeasures," in *Proceedings of the 1st IEEE International Workshop on Sensor Network Protocols and Applications*, 2003.

[5] Y. Xu, J. Heidemann, and D. Estrin, "Geography-informed Energy Conservation for Ad Hoc Routing," in ACM/IEEE International Conference on Mobile Computing and Networking,2001,pp.70-84.

[6] Y. Yu, D. Estrin, and R. Govindan, "Geographical and Energy-Aware Routing: A Recursive Data Dissemination Protocol for Wireless Sensor Networks," 2001.

[7] A. Rezgui and M. Eltoweissy, "_RACER: A Reliable Adaptive Service-Driven Efficient Routing Protocol Suite for Sensor-Actuator Networks," IEEE Transactions on Parallel and Distributed Systems, 2009, vol. 20, no. 5, pp. 607-622.

[8] T. Zahariadis, P. Trakadas, H. Leligou, P. Karkazis, and S. Voliotis, "Implementing a Trust-Aware Routing Protocol in Wireless Sensor Nodes," Developments in E-systems Engineering, 2010, pp. 47-52.

[9] J. Al-Karaki and A. Kamal, "Routing techniques in wireless sensor networks: a survey," IEEE wireless communications, 2004, pp. 1-37.

[10] J. L. X. Li, M. R. Lyu, "Taodv: A trusted aodv routing protocol for mobile ad hoc networks," in *Proceedings of Aerospace Conference*, 2004.

[11] A. Rezgui and M. Eltoweissy, "Tarp: A trust-aware routing protocol for sensor-actuator networks," in *IEEE Internatonal Conference on Mobile Adhoc and Sensor Systems (MASS 2007)*, 8-11 2007.

[12] Z. Cao, J. Hu, Z. Chen, M. Xu, and X. Zhou, "Fbsr: feedback based secure routing protocol for wireless sensor networks," *International Journal of Pervasive Computing and Communications*, 2008.

[13] T. Zahariadis, H. Leligou, P. Karkazis, P. Trakadas, I. Papaefstathiou, C. Vangelatos,

and L. Besson, "Design and implementation of a trust-aware routing protocol for large wsns," *International Journal of Network Security & Its Applications (IJNSA)*, vol. 2, no. 3, Jul. 2010.

[14] J. Al-Karaki and A. Kamal, "Routing techniques in wireless sensor networks: a survey," *Wireless Communications*, vol. 11, no. 6, pp. 6–28, Dec. 2004.

[15] A. Perrig, R. Szewczyk, W. Wen, D. Culler, and J. Tygar, "SPINS: Security protocols for sensor networks," *Wireless Networks Journal (WINET)*, vol. 8, no. 5, pp. 521–534, Sep. 2002.

[16] C. Karlof, N. Sastry, and D.Wagner, "Tinysec: A link layer security architecture for wireless sensor networks," in *Proc. of ACM SenSys 2004*, Nov. 2004.

[17] R. Watro, D. Kong, S. Cuti, C. Gardiner, C. Lynn, and P. Kruus,"Tinypk: securing sensor networks with public key technology," in *Proceedings of the 2nd ACM workshop on Security of ad hoc and sensor networks (SASN '04)*. New York, NY, USA: ACM, 2004, pp. 59–64.

[18] H. Safa, H. Artail, and D. Tabet, "A cluster-based trust-aware routing protocol for mobile ad hoc networks,"*Wirel. Netw.*, vol. 16, no. 4, pp. 969–984, 2010.

[19] W. Gong, Z. You, D. Chen, X. Zhao, M. Gu, and K. Lam, "Trust based routing for misbehavior detection in ad hoc networks," *Journal of Networks*, vol. 5, no. 5, May 2010.

[20] Z. Yan, P. Zhang, and T. Virtanen, "Trust evaluation based security solution in ad hoc networks," in *Proceeding of the 7th Nordic Workshop on Secure IT Systems*, 2003.

[21] J. L. X. Li, M. R. Lyu, "Taodv: A trusted aodv routing protocol for mobile ad hoc networks," in *Proceedings of Aerospace Conference*, 2004.

IMPLEMENTATION OF A PROPOSED 2D DOA ESTIMATION ALGORITHM ON AN FPGA PLATFORM

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Abstract— **Direction of arrival estimation is an important signal parameter in smart antenna which can be used for source localization or source tracking by determining the desired signal location. A new type of estimation algorithm is proposed for the 2-D azimuth and elevation angle estimation problem. FPGA implementation of algorithm can be done using HDL coder of MATLAB.**

Index Terms— DOA, GPS, FPGA

I. OVERVIEW OF DOA ESTIMATION ALGORITHMS

Smart antenna is one of the dynamic research areas in wireless communication systems. The demand for smart antenna increases drastically when dealing with multiuser communication system, which needs to be adaptive, especially in time varying scenarios. Direction of Arrival (DOA) estimation is considered as an important task in smart antennas. It is an important signal parameter which can be used for source localization or source tracking by determining the desired signal location.

Also, it plays a key role in enhancing the performance of adaptive antenna arrays for wireless communication system and other numerous applications in the field of radar and sonar. Therefore, research has been accomplished about DOA estimation during last recent decades. Various DOA estimation methods have been proposed. These methods differ in technique, speed, computational complexity, accuracy and their dependency on the array structure. Different methods have been suggested to enhance the performance of available algorithms including the increase in the accuracy and resolution of DOA estimation algorithms.

According to the underlying methodology, the array signal processing algorithms can be categorized into two classes. The first class is called the non-parametric approach in which the source locations (or the DOA) are estimated by choosing the strongest output power of a spatial filter after sweeping over the space of interest. The advantage of this approach is that no assumption has to be made on the studied signal. The second class is called the parametric approach, in which a nominated model is assumed for the array observations. Once the model is determined, the quantities of interest in the array problem can be determined by choosing the best parameters that fit the model under some optimality criteria.

In general, the direction-of-arrival (DOA) estimation techniques can be broadly classified into conventional beamforming techniques, subspace-based techniques, and maximum likelihood techniques.

A. Classical beamforming

The conventional beamformer works described earlier on the premise that pointing the strongest beam in a particular direction yields the peak power arriving in that direction. In other words, all the degrees of freedom available to the array were used in forming a beam in the required look direction. This works well when there is

only one incoming signal present. Two peaks can be seen at 10^0 and 30^0, but the 30^0 peak is not obvious and are somewhat averaged with the peak at 10^0. In other words, the spread of each peak is large, and if two impinging angles are close to each other, the two peaks may be "blurred" into one pair. In a more general term, although it is simple to implement, the width of the beam associated with a peak and the height of the side lobes, as seen in figure are relatively large; they limit the method's effectiveness when signals arriving from multiple directions and/or sources are present.   This

-100   -80   -60   -40   -20   0   20   40
60   80   100

Angle in degree
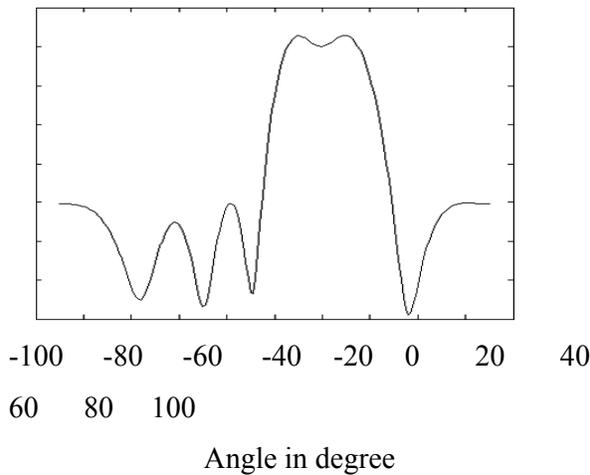
Fig 1: DOA estimation with Classical

Beamformer

technique has poor resolution. Although it is possible to increase the resolution by adding more array elements, it leads to the increase in the numbers of receivers and the amount of storage required for the data.

B. Capon's Beamformer:

The conventional beamformer works well when there is only one incoming signal present. But when there is more than one signal present, the array output power contains signal contributions from the desired angle as well as from the undesired angles. Capon's method overcomes this problem by using the degrees of freedom to form a beam in the look direction and at the same time the nulls in other directions in order to reject other signals. In terms of the array output power, forming nulls in the directions from which other signals arrive can be accomplished by constraining a beam (or at least maintaining unity gain) in the look

direction. Thus, for a particular look direction, Capon's method uses all but one of the degrees of the freedom to minimize the array output power while using the remaining degrees of freedom to constrain the gain in the look direction to be unity and at the same time the nulls in other directions in order to reject other signals. In terms of the array output power, forming nulls in the directions from which other signals arrive can be accomplished by constraining a beam (or at least maintaining unity gain) in the look direction. Thus, for a particular look direction, Capon's method uses all but one of the degrees of the freedom to minimize the array output power while using the remaining degrees of freedom to constrain the gain in the look direction to be unity. It can be seen that in comparison with figure, the peaks at 10° and 30° are much sharper and better separated compared to that of the conventional beamformer. The side peaks or lobes at other angles are also reduced, making them less likely to confuse the interpretation of the output power. The best resolution achieved was 10°. However, this increased resolution comes at the cost of increased computing time or power.

-100   -80   -60   -40   -20   0
20   40   60   80   100

Angle in degree
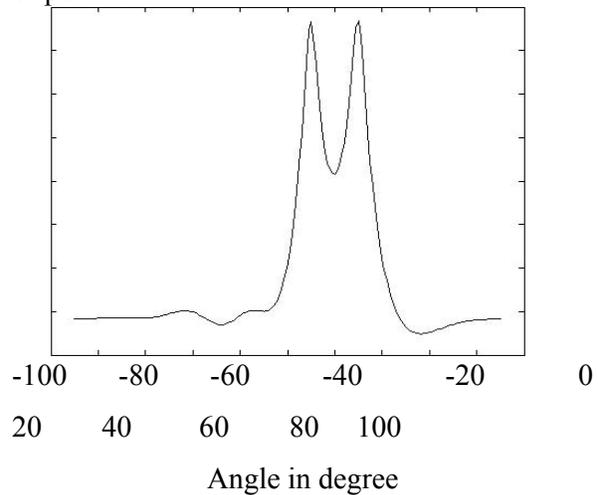
Fig 2: DOA estimation with Capon's

Beamformer

C. Maximum Likelihood Techniques

Maximum likelihood (ML) techniques were some of the first techniques investigated for DOA estimation. Since ML techniques were computationally intensive, they are less.
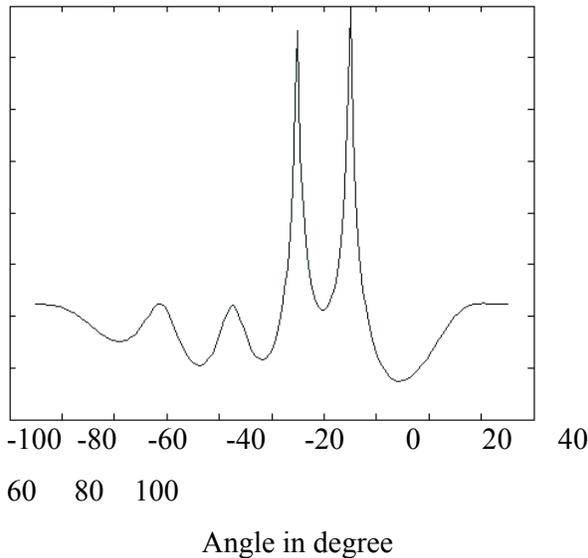
-100 -80 -60 -40 -20 0 20 40
60 80 100

Angle in degree

Fig. 3: DOA estimation with the linear

prediction; the signal impinges at 10° and 30⁰

popular than other techniques. However, in terms of performance, they are superior to other estimators, especially at low SNR

D. MUSIC

MUSIC (Multiple Signal Classification) is one of the earliest proposed and a very popular method for super-resolution direction finding. The DOAs of the multiple incident signals can be estimated by locating the peaks. The *d* largest peaks in the MUSIC spectrum above correspond to the DOAs of the signals impinging on the array.

-100 -80 -60 -40 -20 0 20
40 60 80 100
Angle in degree
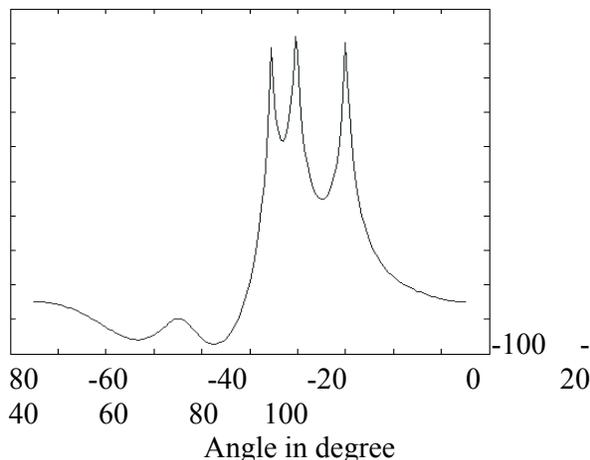
Fig. 4: DOA estimation with MUSIC; the radio

signals impinges at 10°, 20°, and 40°.

E. ESPRIT

100 -80 -60 -40 -20 0 20
40 60 80 100

Angle in degree
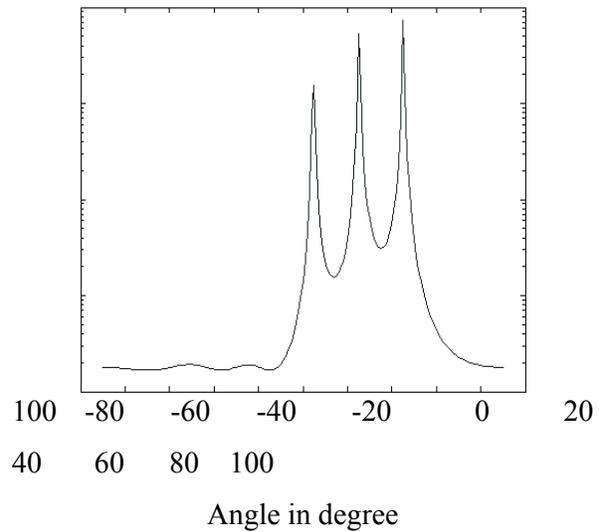
Fig 5: DOA estimation with MUSIC; the radio

signals impinges at 10°, 20°, and 40°.

Due to its simplicity and high resolution capability, ESPRIT has become one of the most popular signals subspace-based DOA estimating schemes. ESPRIT is applicable to array geometries that are composed of two identical sub arrays and is restricted to use with array geometries that exhibit invariances. This requirement, however, is not very prohibitive in practical applications since many of the common array geometries used in practice exhibit these invariances. There are three primary steps in any ESPRIT based DOA estimation algorithm:

1. Signal subspace estimation: Computation of a basis matrix for the estimated signal subspace.

2. Solution of the invariance equation: Solution of an (in general) over determined system of equations, the invariance equation, derived from the basis matrix.

3. DOA estimation: Computation of the eigenvalues of the solution of the invariance equation formed in step 2.

II. PROPOSED METHOD OF DIRECTION OF ARRIVAL ESTIMATION BY ROTATING ADAPTIVE ARRAY ANTENNA PLANE MECHANICALLY

A new technique for 2 D DOA estimation of signals impinging on the array, using mechanical rotation of the array plane by small angle (Azimuth & Elevation) has been proposed for further analysis and discussion.

For an adaptive antenna system, if p users transmit signals from different locations, and each user's signal arrives at the array through multiple paths.

Let LMi denote the number of multipath components of i-th user. We have $\sum_{i=1}^{p} LM_i = p$.

Let's further assume that all of the multi path components for a particular user arrive within a time window which is much less than the channel symbol period for that user, then the input data vector could be expressed as-

$$x(t) = \sum_{i=1}^{p} \sum_{k=1}^{LMi} \alpha_{i,k} a(\theta_{i,k}) s_i(t) + n(t)$$
(1)

Or we can write
$$x(t) = \sum_{i=1}^{p} G_i s_i(t) + n(t)$$
(2)

where $\theta_{i;k}$ is the DOA of the k-th multi path component for the i-th user, $a(\theta_{i;k})$ is the steering vector corresponding to $\theta_{i;k}$, $\alpha_{i;k}$ is the complex amplitude of the k-th multipath component for the i-th user, and G_i is the spatial signature for the i-th user and is given by

$$G_i = \sum_{k=1}^{LMi} \alpha_{i,k} a(\theta_{i,k})$$
(3)

The signal component arriving on nth antenna element at a particular instance of time is given by

$$X_n = A \exp(j2\pi n d \sin\theta \cos\phi / \lambda)$$
(4)
$$Y_n = A \exp(j2\pi n d \sin\theta \sin\phi / \lambda)$$
(5)

Where A= complex amplitude of the signal, φ = Direction of Arrival (DOA) of the signal (Azimuth Angle) (unknown), θ = Direction of Arrival (DOA) of the signal (Elevation Angle) (unknown), d= spacing between antenna elements and λ = wavelength.

Now one can view (4) & (5) as-
$$X_n = A \exp[j2\pi f (d\sin\theta \cos\phi / c)]$$
(6)
$$Y_n = A \exp[j2\pi f (d\sin\theta \sin\phi / c)]$$
(7)

Where f= frequency of the signal and c= velocity of wave.

Now if we mechanically steer the antenna plane by $\delta\varphi$ & $\delta\theta$, then (6) & (7) becomes –

$$X^1{}_n = A \exp[j2\pi f (d\sin\theta \cos(\phi + \delta\phi) / c)]$$
(8)
$$Y^1{}_n = A \exp[j2\pi f (d\sin\theta \sin(\phi + \delta\phi) / c)]$$
(9)
$$X^2{}_n = A \exp[j2\pi f (d\sin(\theta + \delta\theta) \cos\phi / c)]$$
(10)
$$Y^2{}_n = A \exp[j2\pi f (d\sin(\theta + \delta\theta) \sin\phi / c)]$$
(11)

Now taking the frequencies (which can be known by seeing the spectra of the signal) of the signal from (6) and (8), and taking their ratio one could get-

$$\frac{frequency \to X_n}{frequency \to X^1{}_n} = \frac{\cos\phi}{\cos(\phi + \delta\varphi)} = \frac{1}{k} \text{(k is known)}$$

Hence
$$\phi = \tan^{-1}[\frac{\cos\delta\phi - k}{\sin\delta\phi}]$$
(12)

And from (7) & (11), we could get
$$\frac{frequency \to Y_n}{frequency \to Y^2{}_n} = \frac{\sin\theta}{\sin(\theta + \delta\theta)} = \frac{1}{k}$$

$$\theta = \cot^{-1}[\frac{k - \sin\theta}{\cos\delta\theta}]$$
(13)

Now using the simple relation given in (12) & (13) one can determine the unknown DOA (θ & φ) of all incoming signal impinging on the array with suitable algorithm based on (6), (7), (8), (9), (10), (11), (12) and (13).

III. FPGA IMPLEMENTATION PROCEDURE

Basically, an FPGA is a large-scale integrated circuit containing programmable logic blocks, programmable interconnect and programmable input-output blocks. The programmable logic blocks can be programmed to duplicate the functionality of basic logic gates such as AND, OR, XOR, NOT or more complex combinatorial functions such as flip-flops, memory elements, decoders or simple mathematical functions. The programmable input-output blocks at the periphery of the devices provide programmable input and output capabilities. By programming the hierarchy of programmable interconnects, the programmable logic blocks and programmable input-output blocks can be interconnected to perform

whatever logical functions and input-output connections are required. During the past decade, FPGAs have experienced extensive architecture innovations. Many advanced technologies have been applied to FPGA devices that enable the development of higher density and much more powerful devices. Now most FPGA devices also have block RAMs, hardware multipliers and embedded microprocessors besides traditional logic blocks and interconnects. Therefore FPGA devices become extremely well suited to the high-performance real-time signal processing. Defining the behavior of an FPGA chip can be done using a Hardware Description Language (HDL) such as VHDL and Verilog to describe the functions directly. The handwritten code can be guaranteed as optimal by the designer in the sense that one can be sure what is got as an output. However, the optimality of the design is highly related to the experience of the designer which makes the HDL design method difficult for inexperienced designers. Alternatively, defining the behavior of an FPGA can be done using a schematic based design tool, such as the System Generator we mentioned above. The System Generator provides blocks of pre-defined functions, which can be arranged through a graphical user interface. Therefore, the System Generator is easy for designers, especially for persons unexperienced with HDL design method. After defining the behavior using either the HDL method or the schematic method, a technology-mapped net list is generated using an electronic design automation tool. The net list can then be fitted to the actual FPGA architecture using a process called place and route, usually performed by the FPGA Company's proprietary place-and-route software. The user will validate the map, place and route results via timing analysis, simulation, and other verification methodologies. Once the design and validation process is complete, the binary file can be generated (also using the FPGA company's proprietary software) and downloaded to (re)configure the FPGA device. To simplify the design of complex systems in FPGAs, there exist libraries of predefined complex functions and circuits that have been tested and optimized to speed up the design process. These predefined circuits are commonly called IP cores, such as the CORDIC cores and are available from FPGA vendors and third-party IP suppliers. The FPGA device vendors also provide related software to support their chips, such as the Xilinx Integrated Software Environment (ISE). With assistance of these software tools and IP cores, FPGA design is simpler now.

A. MATLAB to FPGA using HDL Coder (TM):

FPGAs provide a good compromise between general purpose processors (GPPs) and application specific integrated circuits (ASICs). GPPs are fully programmable but are less efficient in terms of power and performance; ASICs implement dedicated functionality and show the best power and performance characteristics, but require extremely expensive design validation and implementation cycles. FPGAs are also used for prototyping in ASIC workflows for hardware verification and early software development.

Due to the order of magnitude performance improvement when running high-throughput, high-performance applications, algorithm designers are increasingly using FPGAs to prototype and validate their innovations instead of using traditional processors. However, many of the algorithms are implemented in MATLAB due to the simple-to-use programming model and rich analysis and visualization capabilities. When targeting FPGAs or ASICs, these MATLAB algorithms have to be manually translated to HDL.

For many algorithm developers who are well-versed with software programming paradigms, mastering the FPGA design workflow is a challenge. Unlike software algorithm development, hardware development requires them to *think parallel*. Other obstacles include: learning the VHDL or Verilog language, mastering IDEs from FPGA vendors, and understanding esoteric terms like "multi-cycle path" and "delay balancing".

We will see how we can automatically generate HDL code from MATLAB algorithm, implement the HDL code on an FPGA, and use MATLAB to verify HDL code.

B. MATLAB to Hardware Workflow

The process of translating MATLAB designs to hardware consists of the following steps:
-Model algorithm in MATLAB - use MATLAB to simulate, debug, and iteratively test and optimize the design.

-Generate HDL code - automatically create HDL code for FPGA prototyping.

-Verify HDL code - reuse our MATLAB test bench to verify the generated HDL code.

-Create and verify FPGA prototype - implement and verify design on FPGAs. There are some unique challenges in translating MATLAB to hardware. MATLAB code is procedural and can be highly abstract; it can use floating-point data and has no notion of time. Complex loops can be inferred from matrix operations and toolbox functions. Implementing MATLAB code in hardware involves:

-Converting floating-point MATLAB code to fixed-point MATLAB code with optimized bit widths suitable for efficient hardware generation.

-Identifying and mapping procedural constructs to concurrent area- and speed-optimized hardware operations.

-Introducing the concept of time by adding clocks and clock rates to schedule the operations in hardware.

-Creating resource-shared architectures to implement expensive operators like multipliers and for-loop bodies.

-Mapping large persistent arrays to block RAM in hardware

HDL Coder™ simplifies the above tasks though workflow automation.

Let's look at each workflow step in detail.

1) Fixed-Point Conversion

Signal processing applications are typically implemented using floating-point operations in MATLAB. However, for power, cost, and performance reasons, these algorithms need to be converted to use fixed-point operations when targeting hardware. Fixed-point conversion can be very challenging and time-consuming, typically demanding 25 to 50 percent of the total design and implementation time. The automatic floating-point to fixed-point conversion workflow in HDL Coder™ can greatly simplify and accelerate this conversion process. The floating-point to fixed-point conversion workflow consists of the following steps:

-Verify that the floating-point design is compatible with code generation.

-Propose fixed-point types based on computed ranges, either through the simulation of the testbench or through static analysis that propagates design ranges to compute derived ranges for all the variables.

-Generate fixed-point MATLAB code by applying proposed fixed-point types.

-Verify the generated fixed-point code and compare the numerical accuracy of the generated fixed-point code with the original floating point code. Note that this step is optional. We can skip this step if MATLAB design is already implemented in fixed-point.

2) HDL Code Generation

The HDL Code Generation step generates HDL code from the fixed-point MATLAB code. We can generate either VHDL or Verilog code that implements MATLAB design. In addition to generating synthesizable HDL code, HDL Coder™ also generates various reports, including a traceability report that helps we navigate between MATLAB code and the generated HDL code, and a resource utilization report that shows, at the algorithm level, approximately what hardware resources are needed to implement the design, in terms of adders, multipliers, and RAMs. During code generation, we can specify various optimization options to explore the design space without having to modify our algorithm. In the Design Space Exploration and Optimization Options section below, we can see how we can modify code generation options and optimize your design for speed or area.

3) HDL Verification

Standalone HDL test bench generation:

HDL Coder™ generates VHDL and Verilog test benches from MATLAB scripts for rapid verification of generated HDL code. We can customize an HDL test bench using a variety of options that apply stimuli to the HDL code. We can also generate script files to automate the process of compiling and simulating your code in HDL simulators. These steps help to ensure the results of MATLAB simulation match the results of HDL simulation. HDL Coder™ also works with HDL Verifier to automatically generate two types of cosimulation testbenches:

-HDL cosimulation-based verification works with Mentor Graphics® ModelSim® and QuestaSim®, where MATLAB and HDL simulation happen in lockstep.

-FPGA-in-the-Loop simulation allows running a MATLAB simulation with an FPGA board in

strict synchronization. We can use MATLAB to feed real world data into our design on the FPGA, and ensure that the algorithm will behave as expected when implemented in hardware.

4) HDL Synthesis

Apart from the language-related challenges, programming for FPGAs requires the use of complex EDA tools. Generating a bit stream from the HDL design and programming the FPGA can be daunting tasks. HDL Coder™ provides automation here, by creating project files for Xilinx® and Altera® that are configured with the generated HDL code. We can use the workflow steps to synthesize the HDL code within the MATLAB environment, see the results of synthesis, and iterate on the MATLAB design to improve synthesis results.

a) Design Space Exploration and Optimization Options

HDL Coder™ provides the following optimizations to help we explore the design space trade-offs between area and speed. We can use these options to explore various architectures and trade-offs without having to manually rewrite our algorithm.

b) Speed Optimizations

Pipelining: To improve the design's clock frequency, HDL Coder enables us to insert pipeline registers in various locations within our design. For example, we can insert registers at the design inputs and outputs, and also at the output of a given MATLAB variable in our algorithm.

Distributed Pipelining: HDL Coder also provides an optimization based on retiming to automatically move pipeline registers, we have inserted to maximize clock frequency, by minimizing the delay through combinational paths in our design.

Area Optimizations:

RAM mapping: HDL Coder™ maps matrices to wires or registers in hardware. If persistent matrix variables are mapped to registers, they can take up a large amount of FPGA area. HDL Coder™ automatically maps persistent matrices to block RAM to improve area efficiency. The challenge in mapping MATLAB matrices to block RAM is that block RAM in hardware typically has a limited set of read and writes ports. HDL Coder™ solves this problem by automatically partitioning and scheduling the matrix reads and writes to honor the block RAM's port constraints, while still honoring the other control- and data-dependencies in the design.

Resource sharing: This optimization identifies functionally equivalent multiplier operations in MATLAB code and shares them. We can control the amount of multiplier sharing in the design.

Loop streaming: A MATLAB for-loop creates a FOR_GENERATE loop in VHDL. The body of the loop is replicated as many times in hardware as the number of loop iterations. This results in an inefficient use of area. The loop streaming optimization creates a single hardware instance of the loop body that is time-multiplexed across loop iterations.

Constant multiplier optimization: This design level optimization converts constant multipliers into shift and add operations using canonical signed digit (CSD) techniques.

IV. SIMULATIONS

A. Actual & estimated signals DOA and frequencies
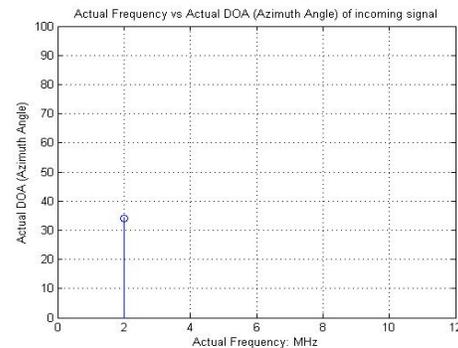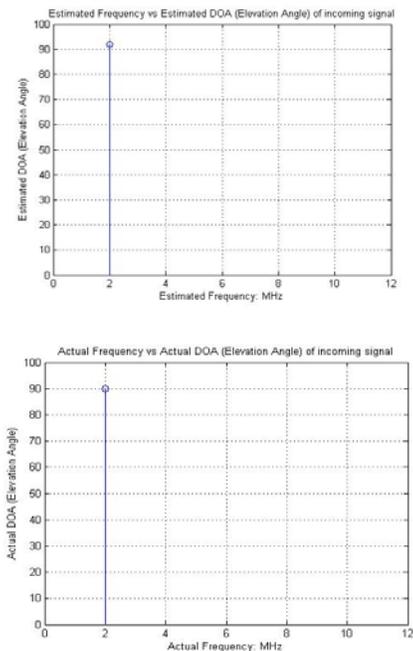
Fig.6-9: Estimated & Actual signals DOA and frequencies

B. *HDL Resource Utilization Report*
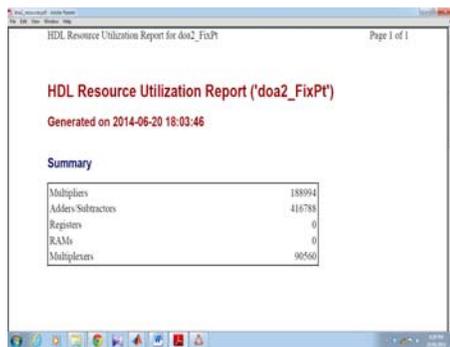
In these simulations **δφ = 1⁰.** Estimated Frequencies and Estimated DOAs are not with the same order as signals are sensed by the array, but after estimating the entire signal space, their plots almost identical as exhibited in fig. (6) to (9).

CONCLUSIONS

FPGA implementation of a proposed 2D DOA estimation algorithm is presented on MATLAB platform. The design employs CORDIC-based processing (array boundary cell) which is well matched to the computational resources of an FPGA. This work points out that spatial processing techniques provide new perspectives in applications related with GPS. The use of 2 D DOA algorithm leads to good solutions where

the interfering and multipath signals need to be canceled. Others scenarios, that made a better representation of GPS problem will be established in order to test the structure. Future studies will work on in the way of have DOA estimators with lower computational burden with 3 dimensional geometry. Also the System Generator programming environment enables the rapid development of heterogeneous systems (processors and FPGAs) while insulating programmers from the frequently complex and error prone programming associated with hardware software partitions. The results indicate successful real time implementation of the proposed and the existing methods.

REFERENCES

[1] Parkinson, B. W., Spilker, J., *Global Positioning System: Theory and Applications*, vol. 1&2, AIAA, 1996.

[2] Zhizhang Chen, Gopal Gokeda, Yiqiang Yu, *Introduction to Direction of Arrival Estimation*, Artech House pub.

[3] Kaplan, E. D., *Understanding GPS Principles and Application*, Arthech House, 1996.

[4] Compton, R. T., *Adaptive Antennas: Concepts and Performance*", Prentice Hall, Englewood Cliffs, NJ, 1988.

[5] Junqueira, C., Ribeiro, M., Romano, J.M.T. *Adaptive Techniques for GPS Systems Enhancement*, 13Th International Technical Meeting of The Satellite Division of the Institute of Navigation set. 2000.

[6] Balanis, *Antenna Theory: Analysis & design*, Wiley publication

[7] T. K. Sarkar, M. C. Wicks, M. Salazar-Palma, R. J. Bonneu, *Smart Antennas*, John Wiley & Sons.

[8] Harry L. Van Trees, *Optimum Array Processing*, John Wiley & Sons.

[9] B. Widrow, P.E. Mantey, L. J. Griffiths, B. B. Goode, *Adaptive Antenna Systems*, IEEE Proc. Vol. 55, No.12, pp. 2143 – 2159, December 1967.

[10] Zhang, Y., Z. Ye, X. Xu, and J. Cui, "Estimation of two-dimensional direction-of-arrival for uncorrelated and coherent signals with low complexity", IET Radar, Sonar & Navigation, Vol. 4, No. 4, 507-509, 2010.

[11]   Ichige, K. and H. Arai, "Implementation of FPGA based fast DOA estimator using unitary MUSIC algorithm [cellular wireless base station applications]," IEEE 58th Vehicular Technology Conference, VTC2003-Fall, Vol. 1, 213-217, 2003.

[12]   Ichige, K. and H. Arai, "Real-time smart antenna system incorporating FPGA-based fast DOA estimator," IEEE 60th Vehicular Technology Conference, VTC2004-Fall, Vol. 1, 160-164, 2004.

[13]   Wang, H. and M. Glesner, "Hardware implementation of smart antenna systems," Adv. Radio Sci., Vol. 4, 185-188, 2006.

[14]   www.mathworks.com

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MATHEMATICAL MODELING ON DROPWISE CONDENSATION

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Abstract:-The phenomenon of dropwise condensation, in which the condensate forms into drops rather than covering the entire cooling surface with a continuous film.Dropwise condensation produces heat transfer coefficients as much as 2 to 10 times greater than those produced by film wise condensation. Hence dropwise condensation is always desirable as it is more effective method of heat transfer than filmwise condensation.Dropwise condensation can be promoted by applying (i) Suitable organic promoter (ii) Thin layer of special metal (iii) Coating with polymer film on condenser surface. Due to successful application of dropwise condensation in small scale industry compound metal films are considerable.Special treatment like chrome plating on condenser surface is required for dropwise condensation.Higly polished surfaces also practice dropwise condensation.A overall heat transfer coefficient model is to be developed for dropwise condensation based on following two parameters.

    (i)   Plating thickness of condenser surface
    (ii)   Surface finishing of plated material.

Correlations for variation of the overall heat transfer coefficient with above two parameters are to be calculated by keeping one as constant and other as a variable. Under Dropwise condensation laboratory conditions, some permanent-type coatings, e.g.,gold, silver,teflon have been found to be effective dropwise condensation promoters. However, the effective lives of some of these promoters have been short, possibly due to surface removal of the coating in service. Furthermore, the effectiveness of permanent type promoters in maintaining dropwise condensation is limited by their low thermal conductivity and the coating thickness.In effect of Condenser Surface with morer polish increased life of brass surface promoted as much as upto 4 times for finishes with numbers 3-0000 grades of emery paper.In experiments it is also noted that very clean and smooth surface actually caused filmwise condensation at first which later changes to dropwise condensation.

Keywords: Overall heat transfer coefficient, Plating Thickness, Surface finish.

I. INTRODUCTION

Whenever a saturated vapour comes in contact with lower temperature surface condensation occurs.There are mainly two mode of condensation processes known as film wise condensation and dropwise condensation. If condensate tends to wet the surface and there by forms a liquid film, then processes of condensation is known as film wise condensation & on the other hand if condensate does not tends to wet the surface, the condensate forms the droplets on the surface and every time fresh surface is exposed to the vapour. By specially treating the condensing surface the contact angle can be changed & the surface become 'non – wettable'.Very high heat transfer rate are reported in dropwise processes due to the good contact between the vapour and surface.[1] Condensation is the change of phase from the vapour state to the liquid or solid state.Condensation plays a major role in the heat rejection parts which generally involve pure substances. The random nucleation, growth and departure of droplets results in a certain size distribution of droplets on the condenser surface.[2] The drop size distribution and the

heat transfer through the individual droplets must be known in order to calculate the heat flux with dropwise condensation. Dropwise condensation has been obtained on these types of surface by one of three methods i) Coating the surface with certain chemical substances called promoters ii) Coating the surface with a solid hydrophobic non-metallic material iii) Coating the surface with a noble metal.The thickness of the promoter layer on the condensation surface also affects the type of condensation, if the layer is too thin filmwise condensation occurs whereas excessive amounts of promoter increases the wettability of the surface.[3]

II DROPWISE CONDENSATION
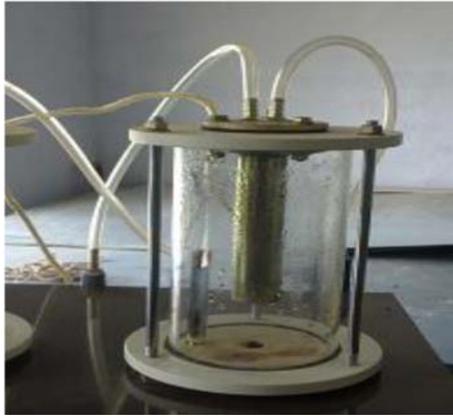
Fig.1 Dropwise Condensation

Dropwise condensation occur when saturated pure vapour comes in contact with the cold surface such has copper tube. When considering surface is contaminated with substance which prevents condensate from the wetting surface ,the vapour will condense in drops instead of a continuous film.Though dropwise condensation would be preferred to filmwise condensation yet it is extremely difficult to achieve or maintain it for long time because most surfaces becomes wetted after being exposed to condensing vapour over a period of time .Dropwise condensation can be obtained under control conditions with the help of certain additives to the condensate and various surfaces coatings but it is commercial viability has not yet been approved for this reason the condensing equipment in use is designed on the basis of filmwise &dropwise condensation.[4]The vapour starts condensing on a surface when the vapour saturation temperature is more than the surface temperature,.the temperature of the condensate formed on the surface is less than its saturation

temperature and it becomes sub-cooled, more vapour will condensate on the exposed surface or on the previously formed condensate as the temperature of the previous condensate is less than the saturation temperature of vapour.[6]

A) Effect of plating thickness :-
Experimentation to study the behavior of a 0.00025-inch thick film of teflon to promotion of dropwise condensation on a 112- inch 0.D. Aluminium tube. The tube was mounted horizontally and both the dropwise and filmwise condensations were studied. It is found that curves of heat transfer coefficients versus vapor to surface temperature drop in dropwise and filmwise condensation lowered as the temperature drop become large. This was caused by the rapid formation of drops which rend to blanket the condenser surface with liquid at high heat fluxes. It is also found that highest heat transfer coefficients were obtained with thinnest teflon film because of the high thermal resistance of teflon. A teflon film thickness of 0.00025-inch provided 12.5 times as thermal resistance as the 0.02-inch thick aluninun wall of the condenser tube and about 3 times more than the condensIng film itself. This shows thar the thickness of the reflon film is an i:nportant parameter and it should be kept at a minimum to imorove the overall perforrance of the tef lon coated condenser tubes. [7]

B) Effect of Surface Roughness :-
Experimentation on dropwise condensation shows that highly polished surfaces produces dropwise condensation in absence of oil or fatty acids. On the other hand filmwise condensation can occur on very rough or very foul surfaces.Polish surface also affect the life of a brass surface..The basic mechanism of maintenance of dropwise condensation in the fact that the condenser surface should be nonwettable to the condensing vapor. All surface treatment, including application
of dropwise preorders, which will cause the surface to become non wettable will be effective in promoting dropwise condensation. Therefore it becomes apparent that the nature of the metal surface and material determines to some extent if a given promoter will be successful in promotion of dropwise condensation The use of different promorers on the same metal surface caused

dropwise condensation fordifferent durations in time.It is noted that using- a mixture of oleic acid and light lubricating oil of a promoter on the surfaces of mirror smooth chrome-plated copper and No 6J emery paper treated stainless steel, the useful promoter life for chrome-plated copper was twice as long as for stainless steel. It is also found that a promoter of some sort was necessary for dropwise condensation that highly polished surface alone will not cause dropwise condensation.[7]

III MATHEMATICAL ANALYSIS

A) Effect of Plating Thickness

In dropwise condensation is modeled including the effect of substrate material. Differentials equations are obtained for temperature distribution in the substrate and the droplet. Since analytical solution of the differential equation system is quite complicated by the known methods, no attempt is made to solve these equations analytically. Instead of solving the differential equations of the drop and the substrate simultaneously, the diffusion equation of the droplet is replaced by the equivalent thermal resistances and these resistances are used as boundary condition for the diffusion equation for the substrate material. Temperature distribution in the substrate material is obtained with finite difference method and the calculations are performed for different substrate materials and for various drop radii. Heat transfer and heat flux are calculated through a single droplet with the use of temperature distribution, then total heat transfer and flux is obtained by integrating the heat transfer through a single drop for the entire drop population. Finally heat transfer coefficient for dropwise condensation is determined by using the total heat flux and average surface temperature of the drop to substrate interface. Previous analytical and theoretical models of dropwise condensation used expressions for the heat transfer through single droplets of specific sizes and then the total heat transfer is determined by integrating over the distribution of sizes. Such an analysis will also be followed here. [6] Following assumptions are made in the analysis of this study :

- The vapor is at uniform temperature.

- Heat transfer from vapor to substrate is carried out only by condensation.
- Substrate material, although it has a finite thickness in typical applications, will be assumed to be a semi-infinite body since its thickness is considerably large for the majority of the droplets on the surface of condensation.
- The area between the droplets can be considered as thermally insulated.

We will first find the heat transfer coefficient inside the condenser under test.for this properties of water are taken at the bulk mean temperature of water e.g. (Twi + Two)/2 where Twi and Two are water inlet & outlet temperature. Following properties are required:

where g = acceleration due to gravity =9.8 m/sec2 =1.27 × 108 m/hr2

L = Length of condenser =160 mm

Overall heat transfer coefficient (U) can be calculated as

$$1/U = [\ 1/hi \ + \ Di/Do \ \ x \ \ 1/ho \ ] \ x \ 4.1868/3600$$

KW/ m²-K - ----------------------------------(1)

Where hi = Inside heat transfer coefficient.

ho = Outside heat transfer coefficient.

Di = Inside diam. Of wall.

Do= Outside diam. of wall.

In order to increase U, ho should be increased

ho = 0.943[Λ x ζ² x g x k³ /   (Ts – Tw) μ x L]^0.25

Where Λ = Heat of evaporation at B.M.T.(Bulk Mean Temp)

ζ = Density of water at B.M.T.

μ = Dynamic viscosity at B.M.T.

Consider a vertical plate of height L and width b maintained at a constant temperature Ts that is exposed to vapor at the saturation temperature Tsat. The downward direction is taken as the positive x-direction with the origin placed at the top of the plate where condensation initiates, as shown in Figure 2. The surface temperature is below the saturation temperature (Ts<Tsat) and thus the vapor condenses on the surface. The liquid film flows downward under

the influence of gravity. The plating thickness δ and thus the mass flow rate of the condensate increases with x as a result of continued condensation on the existing film. Then heat transfer from the vapor to the plate must occur

through the film, which offers resistance to heat transfer. Obviously the thicker the plating, the larger its thermal resistance and thus the lower the rate of heat transfer.The analytical relation for the heat transfer coefficient in film condensation on a vertical plate described above was first developed by Nusselt in 1916. [8]

Then Newton's second law of motion for the volume element shown in Figure 2 in the vertical x-direction can be written as
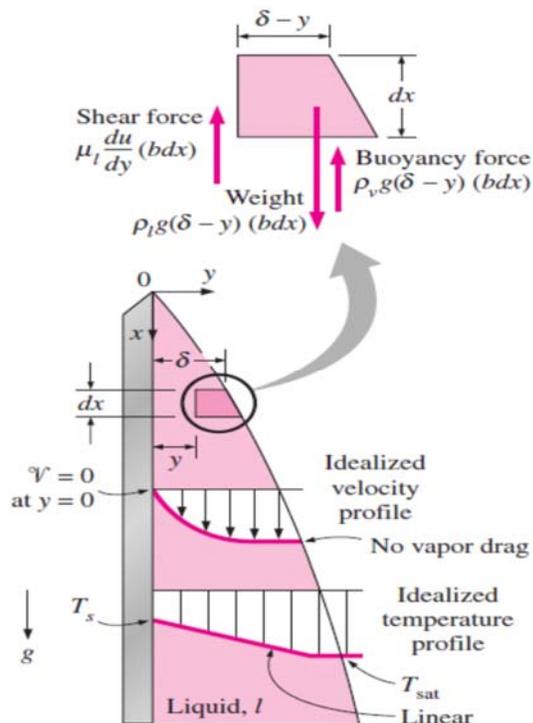

Fig.2 Condensate on vertical plate
Fig.2 The volume element of condensate on a vertical plate considered
In Nusselt's analysis.

$$\sum Fx = ma_x = 0$$

Since the acceleration of the fluid is zero. Noting that the only force acting
downward is the weight of the liquid element, and the forces acting upward are the viscous shear (or fluid friction) force at the left and the buoyancy
force, the force balance on the volume element becomes

$F_{downward\downarrow} = F_{upward\uparrow}$

Weight= viscous shear force + Buoyancy force

$\rho_l g(\boldsymbol{\delta} - y)\,(bdx) = \mu_l\, du/dy\,(bdx) + \rho_v g(\boldsymbol{\delta} - y)(bdx)$

Canceling the plate width b and solving for du/dy gives

$$\frac{du}{dy} = g(\rho l - \rho v)g(\boldsymbol{\delta} - \boldsymbol{y})/\boldsymbol{\mu l}$$

Integrating from y=0 where u=0 (because of the no-slip boundary condition)

To y =y where u=u(y) gives

$U(y) = \dfrac{g(\rho l - \rho v)g}{\mu l}$

$u(y) =$
$\dfrac{g(\rho l - \rho v)g}{\mu l}\left(y\delta - \dfrac{y2}{2}\right)$ (2)

The mass flow rate of the condensate at a location x, where the boundary layer thickness is δ ,is determined from

$M(x) \qquad = \int_A \rho l u(y)dA = \int_{y=0}^{\delta} \rho l u(y)bdy$
(3)

Substituting the u(y) relation from Equation 1 into Eq. 2 gives $\dfrac{m(x)=\ gb\rho l(\rho l - \rho v)\delta^3}{3\mu l}$ (4)

Whose derivative with respect to x is

$$\frac{dm}{dx} = \frac{gb\rho l(\rho l - \rho v)\delta^2}{\mu l}\frac{d\delta}{dx} \qquad (5)$$

which represents the rate of condensation of vapor over a vertical distance dx. The rate of heat transfer from the vapor to the plate through the liquid film is simply equal to the heat released as the vapor is condensed and is expressed as

$$dQ = hfg \, dm = k_1 \, (bdx) \, \frac{\text{Tsat}- \text{Ts}}{\delta} \rightarrow$$

$$\frac{dm}{dx} = \frac{k_l \, b}{h_{fg}} \, \frac{\text{Tsat}- \text{Ts}}{\delta} \qquad (6)$$

Equating Eqs. 4 and 5 for dm· /dx to each other and separating the variables give

$$\delta^3 d\delta = \frac{\mu_l \, k_l (T_{sat}- T_s)}{g\rho_l(\rho_l - \rho_v) \, h_{fg}} \qquad dx$$

(7)

Integrating from x=0 where δ =0 (the top of the plate) to x=x where

$$\delta = \delta(x)$$

the liquid film thickness at any location x is determined to be

$$\delta(x) = \left[\frac{4 \, \mu_l \, k_l \, (\text{Tsat} - \text{Ts}) \, x}{g\rho_l(\rho_l - \rho_v) \, h_{fg}}\right]^{1\backslash 4}$$

(8)

The heat transfer rate from the vapor to the plate at a location x can be
expressed as

$$q_x = h_x(\text{Tsat} - \text{Ts})=k_l \, \frac{\text{Tsat}- \text{Ts}}{\delta} \rightarrow h_x = \frac{kl}{\delta(x)}$$

(9)

Substituting the δ(x)expression from Eq. 7, the local heat transfer coefficient hxis determined to be

$1/U = [1/hi + Di/Do \times 1/ho + \partial/K] \times 4.1868/3600$
KW/ m²-K   (10)

B) Effect of Surface Roughness :-

In conclusion, we have shown that for relatively low humidity capillary forces are present in the case of smooth surfaces, and surpasses in magnitude any dispersion and electrostatic forces. In addition, an enormous decrease in the capillary force was observed by increasing the roughness amplitude a few nanometers in the range ∼1-10 nm. Considering the rapid fall off in the capillary force and the two limits (a smooth limit where the whole surface contribute to the capillary force, and a rough limit where only a single or a few asperities contribute), the crossover regime might in turn depend on the

contact angle and any lateral roughness features. Both could be an intersecting direction for further study of this phenomenon in the design MEMS (micro electromechanical systems) if stiction poses a problem. The total adhesion force can be divided into a capillary force and an interfacial tension force due to surface tension acting tangentially to the interface along the contact line with the solid body.The Laplace pressure, while ignoring contributions from surface tension.

$Fup= 4\pi \, v \, Rh \, Cos\Theta.$ (11)

Where ν = Liquid vapour pressure,

Rs = Surface roughness,

Θ = contact angle of vapour with condenser surface.

 For the contact angle of water onto Au surfaces we obtain for Θ =70°,Rs=50μm, $Fup=1.5X10^4$ nN It appears that the smooth limit is reached for the Au/mica film. For the roughest films the values found are up to ten times higher than that of a single asperity, indicating a capillary interaction of a multitude of asperities

For a increase in 100% roughness, capillary force reduces up to 1/10 times applicable only after 60% rise in roughness. [5]This will effect condensation in the same manner. From this result alongwith equation (1) and (11) we can write as

$1/U = Rm/10[1/hi + Di/Do \times 1/ho] \times 4.1868/3600$
KW/ m²-K - ---------------------------------- (I)

Where Rm= Number of times of original roughness value.

IV. CONCLUSION

In this paper through mathematical mode finally observed that the heat transfer coefficient (h W/m2K) associated with dropwise condensation is decreases with increase in plating thickness of coatings. It can be calculated depending on the formula with respect to plating thickness. The drop wise condensation is also affected by roughness of coated surface. In mathematical mode finally it is observed that the heat transfer coefficient (h W/m2K) associated with dropwise condensation is decreases with increase in roughness of coated plate. Plating thickness of coatings. It can be calculated depending on the formula with respect to plating thickness.

      And also this paper suggest that whenever the requirement of condensation is

more ,the surface should be with minimum plating thickness and with minimum value of surface roughness.

REFERENCES

[1] Saurabh pandey, Dropwise and filmwise condensation, International Journal of Scientific & Engineering Research, Volume 3, Issue 4, April-2012 ISSN 2229-5518.

[2] M. Rama Narasimha Reddy, Dr M.Yohan, K.Harshavardhan Reddy, Heat transfer coefficient through dropwise and filmwise condensation apparatus, International Journal of Scientific and Research Publications, Volume 2, Issue 12, December 2012 1 ISSN 2250-3153

[3] Gagan Deep Bansal, Sameer Khandekar, and K. Muralidhar, Measurement of heat transfer during dropwise condensation of water on polyethylene, Nanoscale and Microscale Thermophysical Engineering, 13: 184–201, 2009.

[4]Dr.S.Alec Watson,Nickel Development Institute,Watson Consultancy Services,Solihull,England, 1989.

[5] P.J. van Zwol, G. Palasantzas* and J. Th. M. De Hosson, Influence of random roughness on the adhesion between metal surfaces due to capillary condensation, Applied Physics letters 91, 101905 _2007.

[6] Cecil E. Kirby, Promotion of dropwise condensation of ethyl alcohol,methyl alcohol and a roethylene,National Aeronautics and Space Administration Washington,D.C.July 1971.

[7] S. C. Garg, Ph.D., Technical Note N-1041The effect of coating and surfaces on dropwise co ndensation July 1969

[8]Yunus A.Cengel,Reference book on Heat Transfer.

EXPERIMENTAL MEASUREMENT AND COMPARISON OF SHAFT VOLTAGE AND THE BEARING CURRENT IN MULTILEVEL INVERTER FED THREE PHASE INDUCTION MOTOR

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Abstract—It is known that by using the inverter to generate three phase AC supply from a single DC source it introduces common mode (CM) voltage at the stator star point of the IM with respect to general ground (gnd). In addition high frequency switching noise pulses will be induced due to the fast switching of the inverter devices at the IM supply lines. This CM voltage and high frequency switching noise pulses are harmful and will be responsible for the flow of current through the bearing to the general gnd and also creates electromagnetic interference (EMI) problems respectively. The flow of bearing current leads to premature bearing failures and the EMI affects the communication and measuring systems / circuits. The influence of different parameters of a variable speed drive system on the phenomena of inverter-induced bearing currents has been studied earlier under exactly the same conditions on inverter-operated A.C motor. Detailed modeling may not always be possible with practical Applications in the field, where many parameters might be unknown. Therefore, this paper presents experimental methods of measurement of the common mode voltage,shaft voltage and bearing current for a modified 3- phase squirrel cage induction motor (IM) connected to an neutral point clamped (NPC) inverter bridge. Experiments have been carried out on 2-level and multi-level inverter fed IM drives using space vector modulation (SVM) scheme. Microcontroller was used to generate SVM pulses along with other associated electronic interface circuits to operate the inverter bridges. Necessary converter circuits were fabricated and tested for giving the proper DC voltage supply voltage to the inverter bridge. Standard current probe, LISN and high frequency 4-channel Digital Signal Oscilloscope (DSO) with differential probes and were used to measure the shaft voltage, bearing current& other parameters. 4 Channel Mixed Signal Oscilloscope (MSO) was used to record the digital signals from the μcontroller. As per Federal Communications Commission (FCC) and Special Committee on Radio Interference (CISPR) standard, graphs were plotted showing Frequency vs Common mode voltage,shaft voltage in dBμV and the bearing current in dBμA using the signal analysis software.

Index Terms—CM voltage, shaft voltage, bearing current, SVM scheme, 2-level inverter, multilevel inverter, induction motor.

I. INTRODUCTION

The phenomena of bearing currents in adjustable speed drive systems using Converter-Inverter is due to the existence Of Common Mode (CM) voltage and also by fast switching ON and OFF of power electronic devices used in inverters have been reported for almost a decade [1]–[8]. Shaft voltages and their resulting currents were recognized by Alger in the 1920's. The asymmetrical flux, through the arbour line loop (the shaft loop), induces CM voltage. In 1996, Chen and Erdman identified the capacitive CM voltage between stator and rotor due to a switch-mode variable speed motor drive. Since 2000, the number of papers dealing with capacitive electrical machining (EDM) and its consequence (the lifetime reduction of bearing/bearing failure) has increased. Annette Muetze et al. [8] reports that the high-frequency (HF) components of the common mode voltage interact with capacitances of the motor that are not of influence at line operation, thereby possibly generating inverter-induced bearing currents. The induced bearing currents can be from influence of CM voltage on the shaft, the ground currents due to CM voltage and the capacitance between stator and rotor windings with high dv/dt at the input to the IM terminals [9]–[11]. D. Busse, J. Erdman, R. Kerkman, D. Schlegel, and G. Skibinski [12] have explained about the characteristics of shaft voltage induced in the IM due to converter-inverter adjustable speed drive system. All motors have some level of shaft voltage. Above a certain level, shaft voltage is a failure indicator of the Bearing.

II. COMMON MODE VOLTAGE IN INVERTER DRIVEN AC MACHINE

A. Common Mode Voltage

In a three –phase AC system, the common-mode voltage can be defined as the voltage difference between the power source and the neutral point of a three-phase load. If the load is an AC motor, the neutral point of the load means the stator neutral of the motor. It is important to define the common-mode voltage in mathematical terms in order to compare its characteristics among different types of source and load combinations.

In three-phase AC loads, the phase to ground voltages (Va-G, Vb-G and Vc-G) can be written as the sum of the voltages to the neutral point of the load and the neutral point of the load to system ground (VN-G). As per the definition, the common mode voltage is the voltage across the neutral point of the load and the system ground. Since in a balanced system, the sum of all three phase-to-neutral voltages is zero, the voltage from the neutral to ground (common-mode voltage) can be defined in terms of phase discharge ground voltage as shown below

$$V_{a-G} = V_{a-N} + V_{N-G}$$
$$V_{b-G} = V_{b-N} + V_{N-G}$$

and $$V_{c-G} = V_{c-N} + V_{N-G}$$

$$V_{a-N} + V_{b-N} + V_{c-N} = 0 \qquad (1)$$

from above, $$V_{N-G} = \frac{V_{a-G} + V_{b-G} + V_{c-G}}{3}$$

In equation (1), it is assumed that the load is balanced so that the sum of all three phase-to-neutral voltages is Zero ($\sum Va,b,c\text{-}N=0$).If the source voltage is assumed to be balanced and ideal, then the sum of all three phase-to-ground voltages is zero ($\sum Va,b,c\text{-}G=0$).In that case, $V_{N\text{-}G}$ will be zero from equation (1).However, in the case of an inverter-driven AC machine, there exists a common-mode voltage because the voltage source inverter does not constitute an ideal balanced source.

$$V_{com} = V_{N-G} \approx V_{N-M} = \frac{V_{U-M} + V_{V-M} + V_{W-M}}{3}$$
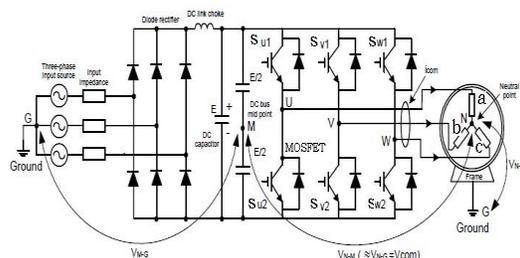
Fig.1 shows a typical 2-level voltage source inverter-fed AC machine.

In an inverter-driven system, the common mode voltage (*VCOM* or *VN-G*) can also be defined as the voltage across the stator neutral (*N*) and the *DC* bus mid-point (*M*) because from a high-frequency viewpoint, the *DC* bus mid-point (*M*) is same as the electrical ground (*G*) of the system. Using this definition, the common-mode voltage can be redefined as shown in equation (2). This definition would then be valid for 3-level inverters as well.

In equation (2), it should be noted that the source voltage nomenclature has been changed from Va,b,c-G to Vu,v,w-M to reflect the fact that the source now is the voltage source inverter. The common mode current (icom) is defined as the instantaneous sum-total of all the currents flowing through the output conductors. Stray capacitances of the motor cable and inside the motor are the paths of this current, and a source of EMI noise problems. Generally PWM inverter gives the two levels of output voltages which are not closer to sinusoidal. In order to minimize the CM voltage and to achieve the high quality output voltage which is closer to sinusoidal and also to get lower %THD, multilevel inverter topologies are preferred.

B. Multi-level Inverter

Several multilevel inverter topologies and modulation technologies have been developed and applied to high power and high voltage systems. The main motivation for phase inverter is 27 (mp where "m" is the level and "p" is the no. of phases) and for 5- level inverter it is 125 and so on.

Presently there are three kinds of multilevel inverters: (1) Neutral Point Clamped inverter (NPC) (2) Flying Capacitor inverter and (3) Cascaded inverter. The proposed work investigates the experimental evaluation of 2-level, Multi-level (3-level , 5-level) inverters for the speed control of induction motor, identification, measurement of CM voltage, shaft voltage and the bearing current using Space Vector Modulation (SVM) method.

The inverter is built using the MOSFET devices, DC link capacitors and the clamping diodes.

For the proposed work Neutral point clamped (NPC) multi level inverter structure is used. In multilevel voltage source inverters, SVM methodologies have the advantages of increased inverter output voltage when compared to sine triangle pulse width modulation (SPWM) method. One of the most important advantages of the SVM is that the gating signal of the power devices can be easily programmed using Microcontrollers/digital signal processor (DSP). Also, SVM offers improved dc bus utilization, reduced commutation losses and lower total harmonic distortion.

C. Space Vector Modulation

In 2- level and multilevel inverters using SVM methodologies, identifies each switching state as a point in complex (∝,β) plane. Then a reference vector rotating in (∝,β) plane at the fundamental frequency is sampled within each switching period, and the nearest three inverter switching states are selected with duty cycles calculated to achieve the same volt-second average as the sampled reference vector. This directly controls the inverter line-to-line voltages, and implicitly develops the phase leg voltages.

III. EXPERIMENTAL RESULTS
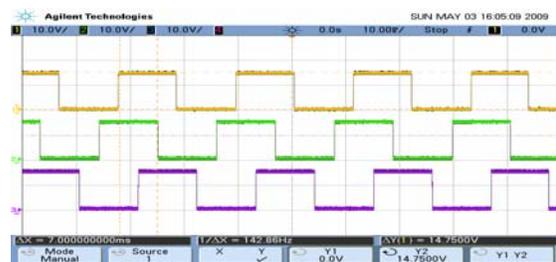
Fig. 2. Micro-controller output for 2- level inverter

Fig. 3. Gating signal generation (switching pattern) for 3-level inverter
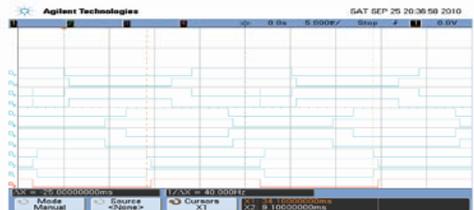
Fig. 4. Gating signals of μ-controller output for NPC 5-Level NPC inverter(only for top side devices).
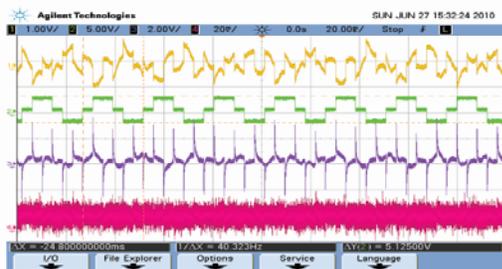
Fig. 5. DSO recorded waveforms(2-level Inverter)
Ch 1:   200 : 1 Star point of IM to Gnd.
Ch 2:   200 : 1 Line voltage to IM.
Ch 3:   20 : 1 Vector sum of Ph current in terms of voltage.
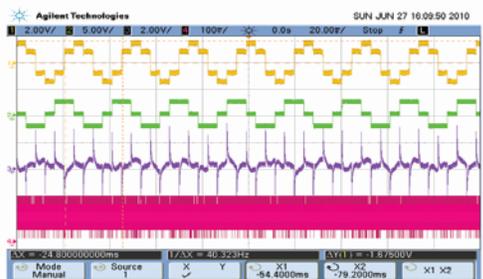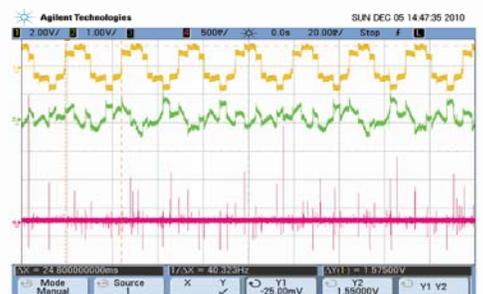Ch 4   1 : 1 Ph current in terms of voltage.

Fig. 6. DSO recorded waveforms(2-level inverter)
Ch 1:   200 : 1 Phase voltage to IM.
Ch 2:   200 : 1 Line voltage to IM.
Ch 3:   20 : 1 Vector sum of current in terms of voltage.
Ch 4:   1 : 1 One phase current in terms of voltage.

Fig. 7. DSO Recorded waveform. (3-level inverter)
Ch.1.200 : 1 Phase voltage.(2v/Div)
Ch 2:   200 : 1 common mode voltage (1v/Div) Ch
3:    1 : 1 Bearing current using the current probe
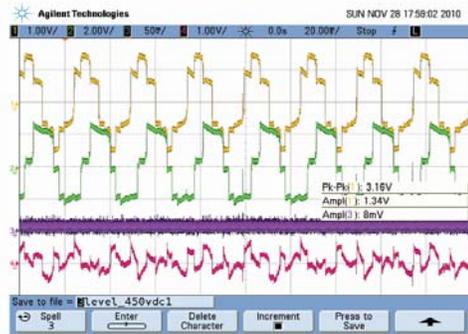
Fig. 8. DSO recorded waveform.(3-level inverter)
Ch 1:   200 : 1 Phase voltage
Ch 2:   200 : 1 Line voltage Ch3: 1: 1 Vector sum of ph. current
Ch 4:   200 : 1 Common mode voltage
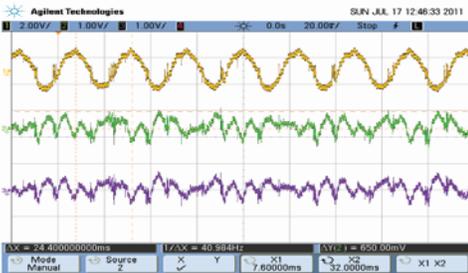
Fig. 9, DSO Recorded waveform (5-level NPC Inverter)
Ch 1:   200 : 1 Phase voltage (2V/div)
Ch 2:   200 : 1 CM voltage   (1V/div)
Ch 3:   200 : 1 Shaft voltage(1V/div)
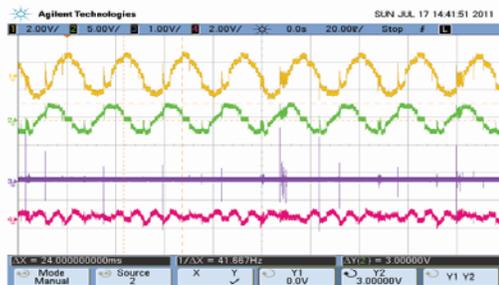
Fig. 10. DSO Recorded waveform (5-level NPC inverter)
Ch 1:   200 : 1 Phase Voltage
Ch 2:   200 : 1 Line Voltage
Ch 3:   1 : 1 Sum of Ph. Current in terms of voltage
Ch 4:   200 : 1 CM voltage
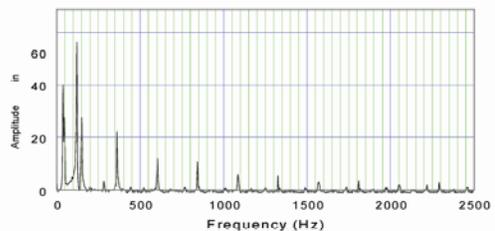
Fig. 11. FFT of Common mode voltage of IM. (20msec/Div,2-level inverter)

Fig. 12. FFT of CM voltage of IM (3-level inverter)
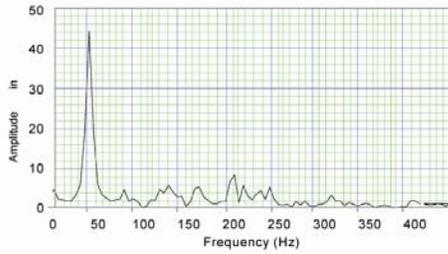
Fig. 13. Expanded view of FFT of CM voltage (3-level inverter)

Fig. 19. FFT of im shaft voltage in Volts(5-level NPC inverter)

Fig. 14. FFT of CM voltage of IM in dB µV(3-level inverter)
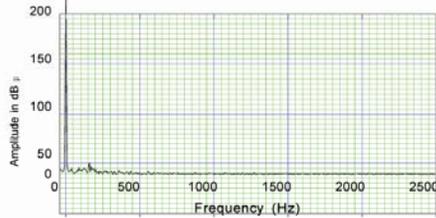
Fig. 20. FFT of IM shaft voltage (3-level inverter)
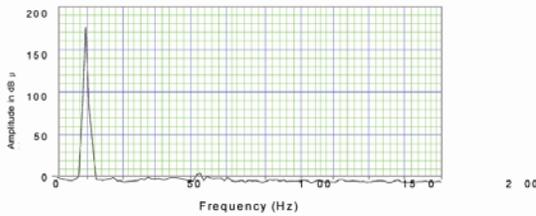
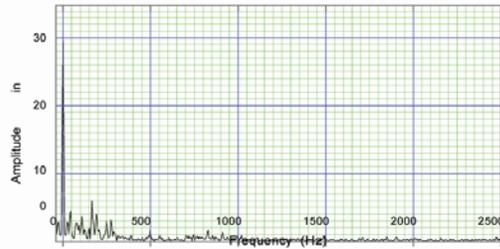Fig. 15. FFT of CM voltage of IM in dBµV (Expanded view, 3-level inverter)
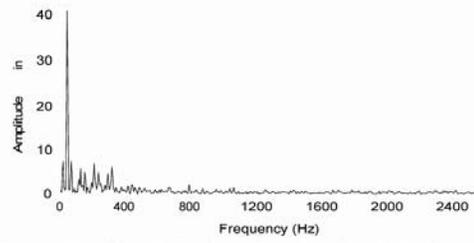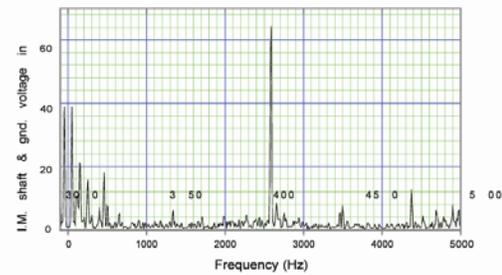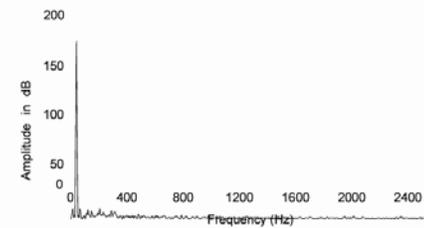

Fig 21. FFT of I.M. shaft voltage (2-level inverter)

Fig. 16. FFT of Common mode voltage of IM in volts (5- level NPC inverter)

Fig. 22. FFT of Shaft voltage in dB µV (5-level NPC inverter)

Fig. 17. FFT of cm voltage of IM (X-Y expanded, 5-level NPC inverter)

Fig. 23. FFT of Shaft voltage in dB µV (3-level inverter)
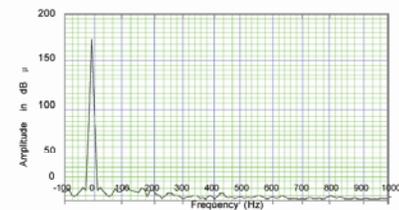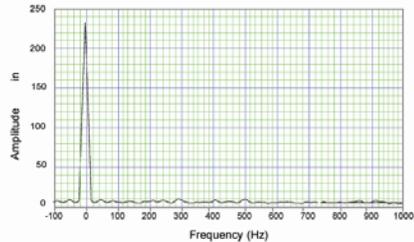
Fig 18.FFTof common mode voltage of IM in DBμV(5-level NPC inverter)

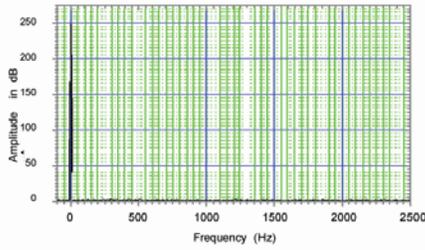Fig. 24. FFT of shaft voltage in dBµV (2-level inverter)

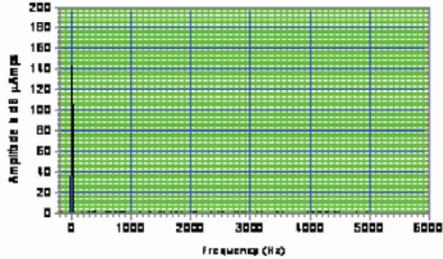Fig. 25. FFT of Bearing current in µA(5-level NPC Inverter)

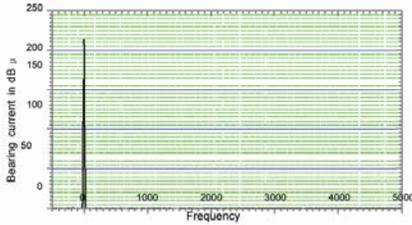Fig. 26. FFT of bearing current in dBµA (3-level Inverter)

Fig. 27. FFT of bearing current in dBµA (2-level Inverter)

TABLE I: THE FFT OF COMMON MODE VOLTAGE, SHAFT VOLTAGE AND THE BEARING CURRENT IN INVERTER FED INDUCTION MOTOR

Sl No.	Inverter Level	FFT of CM Voltage		
		Frequency in Hz	Value in volts	Value in dBµV
1.	2- Level Inverter	Fundamental frequency(40) 120 200 280 440	49 10 8 5 3	180 14 12 11 5
2.	3-Level Inverter	Fundamental frequency(40) 120 200 280 440	42 2 4 3 2	170 6 5 4 3
3	5- Level Inverter	Fundamental frequency(40) 120 200 280 440	36 1 2.5 3 1	160 1 1.5 2 0.8

Sl No.	Inverter Level	FFT of Shaft Voltage with respect to gnd.		
		Frequency in Hz	Value in volts	Value in dBµV
1.	2- Level Inverter	Fundamental frequency(40) 120 200 280 440	64 12 5 6 14	220 2 4 5 2.5

2.	3-Level Inverter	Fundamental frequency(40) 120 200 280 440	45 9 8 6 5	170 13 10 5 6
3	5- Level Inverter	Fundamental frequency(40) 120 200 280 440	38 5 7 4 1.5	155 10 9 7 2

Sl No.	Inverter Level	Current flow from rotor shaft to the gnd through the Bearing (Bearing Current)	
		Frequency in Hz	Value in dBµA
1.	2- Level Inverter	Fundamental frequency(40) 120 200 280 440	220 1.5 1.3 1.2 1.1
2.	3-Level Inverter	Fundamental frequency(40) 120 200 280 440	145 2.2 2.1 1.9 1.9 (Hz)
3	5- Level Inverter	Fundamental frequency(40) 120 200 280 440	135 1.2 0.9 0.8 0.6

IV. CONCLUSION

This work proposes a simple and efficient SVM method that uses only outermost active voltage vectors. Due to these reasons the proposed SVM is computationally very simple and efficient. The research work presented in this paper is about the identification and the experimental measurement of the Common Mode Voltage in 2-level, 3-level and the 5-level (NPC) inverter fed induction motor drive and the technique of SVM scheme. This work also discusses identification as well as the experimental measurement of the rotor shaft voltage and the bearing current that is present in the modified squirrel cage three phase inverter fed induction motor drive. Figures 2, 3 and 4 shows the gating signal generation to the inverter circuits using micro-controller. Figures 5 to 10 shows the DSO recorded wave forms of the 2-level and multilevel Inverters. Figures 11to 27 shows the FFT results of the DSO Recorded waveforms using signal analysis software. The table-1 shows the comparison of the FFT results of the various parameters. It is observed experimentally by measuring the CM voltage and analyzing the same with FFT analysis using the Signal Analysis software that the 5-level inverters generates less CM voltage,

Shaft voltage and the Bearing current when compared to 3-level and 2- level inverter(Table-1).

REFERENCES

[1] S. Chen, T. A. Lipo, and D. Fitzgerald, "Modelling of bearing currents in inverter drives," *IEEE Trans. Ind. Appl*", vol. 32, no. 1, pp. 21–32, Jan./Feb. 1996.

[2] S. Chen, "Bearing current, EMI and soft switching in induction motor drives," Ph.D. dissertation, Univ. Michigan, Ann Arbor, MI, 1996.

[3] J. Erdman, R. Kerkman, and D. Schlegel, "Effect of PWM inverters on AC motor bearing currents and shaft voltages," *IEEE Trans. Ind". Appl*", vol. 32, no. 2, pp. 250–259, Mar./Apr. 1996.

[4] D. Busse, J. Erdman, R. Kerkman, D. Schlegel, and G. Skibinski, "The effect of PWM voltage source inverters on the mechanical performance of rolling bearings," *IEEE Trans. Ind. Appl*", vol. 33, no. 2, pp. 567–576, Mar./Apr. 1997.

[5] D. Busse, J. Erdman, R. Kerkman, and D. Schlegel, "Bearing currents and their relationship to PWM drives," *IEEE Trans. Power Electron*", vol. 12, no. 2, pp. 243–252, Mar. 1997.

[6] R. F. Schiferl and M. J. Melfi, "Bearing current remediation options," *IEEE Ind. Appl. Mag*", vol. 10, no. 4, pp. 40–50, Jul./Aug. 2004.

[7] A. Muetze and A. Binder, "Don't lose your bearings—Mitigation techniques for bearing currents in inverter-supplied drive systems," *IEEE Ind.Appl. Mag*", vol. 12, no. 4, pp. 22–31, Jul./Aug. 2006.

[8] A. Muetze and A. Binder, "Systematic approach to bearing current evaluation in variable speed drive systems," *Eur. Trans. Electr. Power*", vol. 15, no. 3, pp. 217–227, 2005.

[9] A. Muetze and A. Binder, "Calculation of circulating bearing currents in machines of inverter-based drive systems," *IEEE Trans. Ind. Electron*", vol. 54, no. 2, pp. 935–938, Apr. 2007.
Z. Krzemien, "Bearing currents in induction motors supplied with power from PWM inverters," in *Proc. ICEM*", Istanbul, Turkey, pp. 592–596, 1998.

[10] A. Binder, R. Aust, and A. Schrepfer, "Bearing currents—A danger to inverter-fed AC-motors?" *Iron Steel Eng*", vol. 76, pp. 47–52, Jul. 99.

[11] D. Busse, J. Erdman, R. Kerkman, D. Schlegel, and G. Skibinski, "Characteristics of shaft voltage and bearing currents," *IEEE Ind. Appl. Mag*", vol. 3, no. 6, pp. 21–32, Nov./Dec. 1997

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